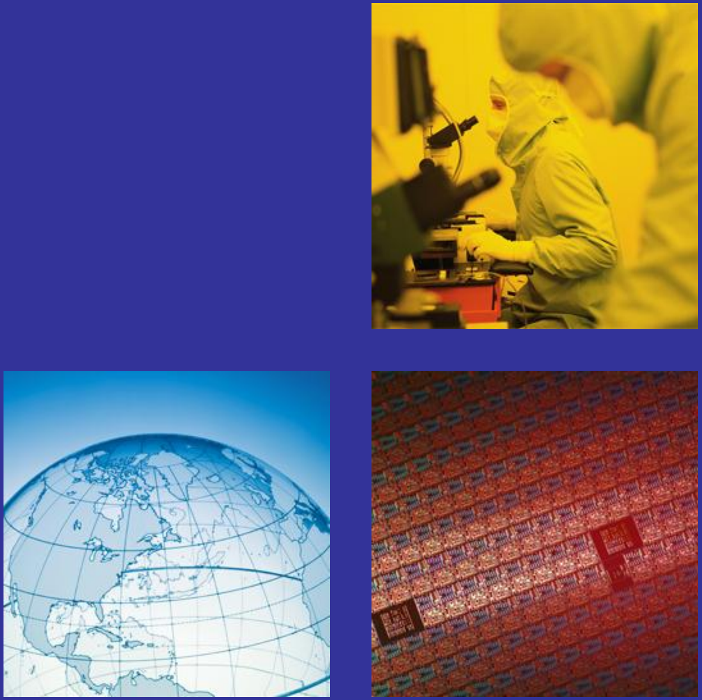
Accelerating the next technology revolution

Doping trends and chemistries for advanced devices



Where can the Chemists contribute for next generation devices?

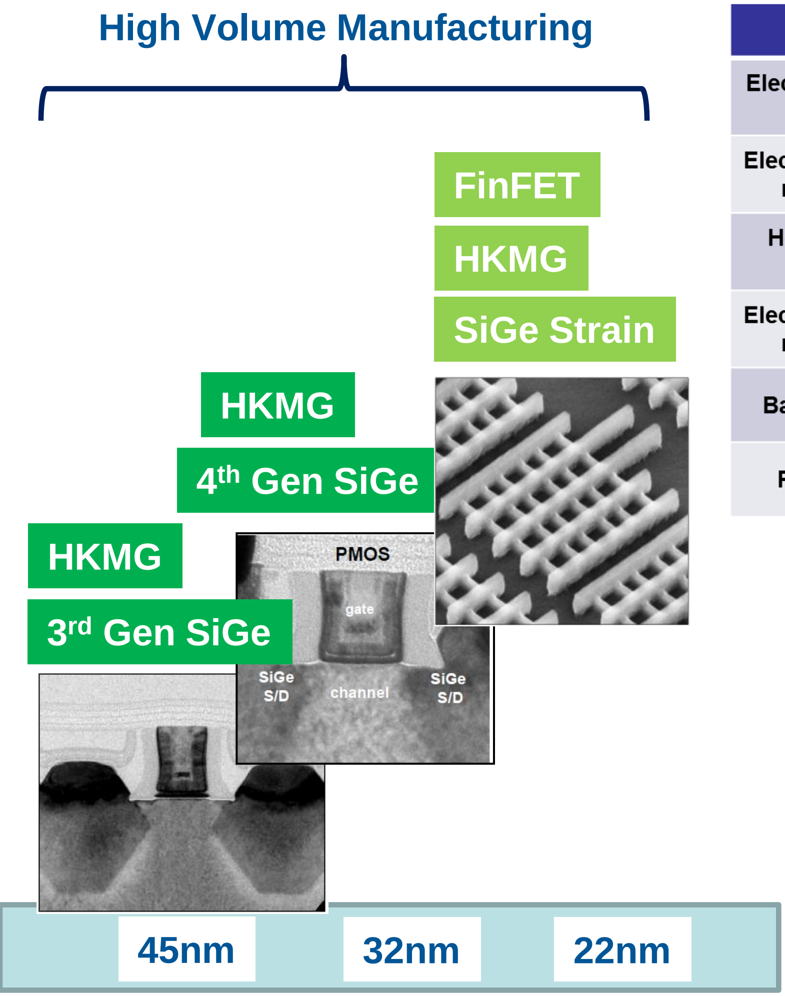
- New materials and structures require new chemistries
  →FINFETs & high mobility channels may require <u>M</u>ono-<u>L</u>ayer <u>D</u>oping

  →MLD

Outline

- Junction Doping & Scaling Challenges
- Monolayer Doping Process Technology
  - MLD Process Development
  - MLD FinFET Demonstration
  - MLD Prospect & Scalability
- Summary

Next generation FinFETs Require New Materials/Chemistries



High Volume Manufacturing

FinFET
HKMG
SiGe Strain

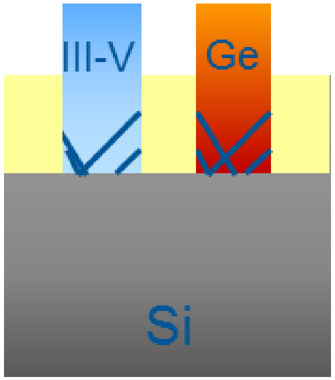
HKMG
4th Gen SiGe

HKMG
3rd Gen SiGe

45nm
32nm
22nm

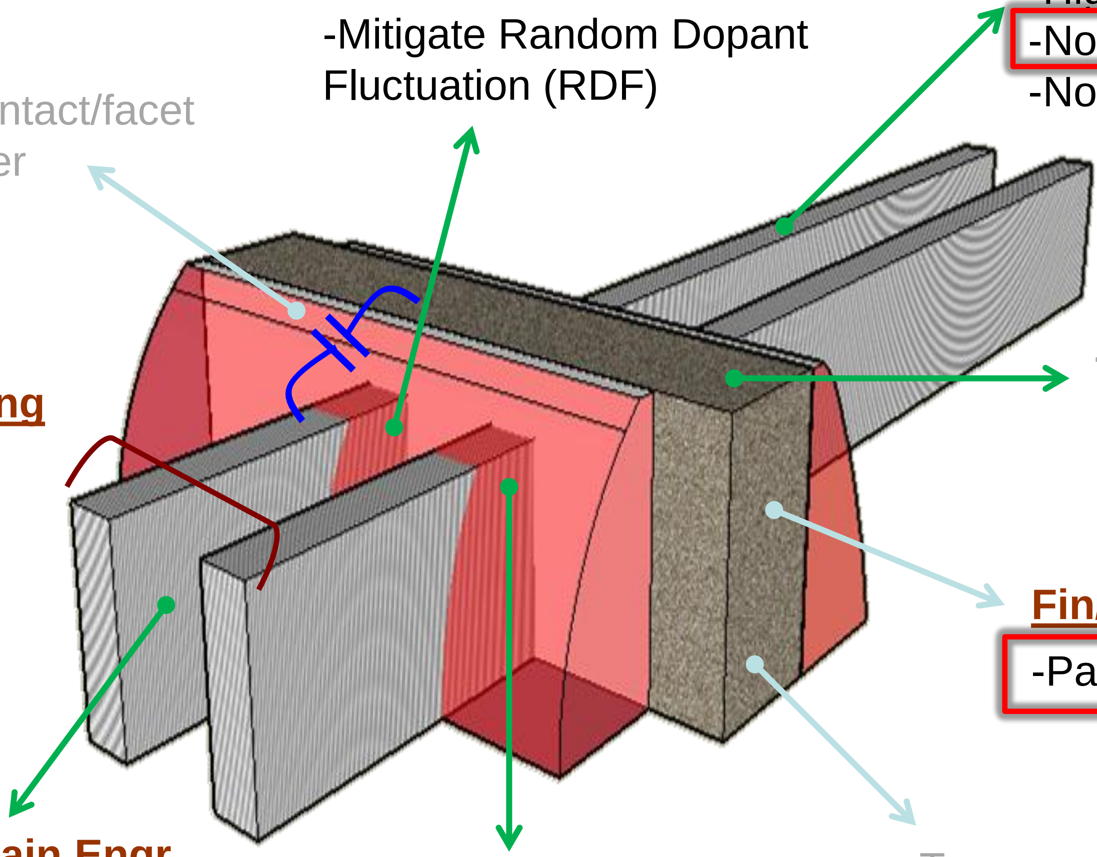
	Si	Ge	GaAs	InAs	InP	InSb
Electron mobility (cm^2/Vs)	1600	3900	9200	40000	5400	77000
Electron effective mass (/m$_o$)	m_t : 0.19 m_l : 0.916	m_t : 0.082 m_l : 1.467	0.067	0.023	0.082	0.014
Hole mobility (cm^2/Vs)	430	1900	400	500	200	850
Electron effective mass (/m$_o$)	m_{HH} : 0.49 m_{LH} : 0.16	m_{HH} : 0.28 m_{LH} : 0.044	m_{HH} : 0.45 m_{LH} : 0.082	m_{HH} : 0.57 m_{LH} : 0.35	m_{HH} : 0.45 m_{LH} : 0.12	m_{HH} : 0.44 m_{LH} : 0.016
Band gap (eV)	1.12	0.66	1.42	0.36	1.34	0.17
Permittivity	11.8	16	12	14.8	12.6	17

1. 3D FIN geometry with high μ materials
2. High μ materials require low thermal budgets
3. Need low temperature 3D doping technique



FinFET / Tri-Gate Scaling Challenges

Enabling Non-Planar Scaling for 11nm Node and Beyond



Capacitance

-Fringe to contact/facet
-Low-k spacer

Variability

-Mitigate Random Dopant Fluctuation (RDF)

Contact Resistance

-High Rco/Rch ratio
-Novel 3D Doping
-Novel Silicide

Fin / Pitch Scaling

-2nd gen scaling (beyond 14nm)

Gate Stack

-Higher-k dielectric
-MG WF Tuning

Fin/Gate Fidelity

-Patterning & Etch

Fin/Channel Strain Engr

-High Mobility Channel
-Dual epi on Fins

Rext Limitations

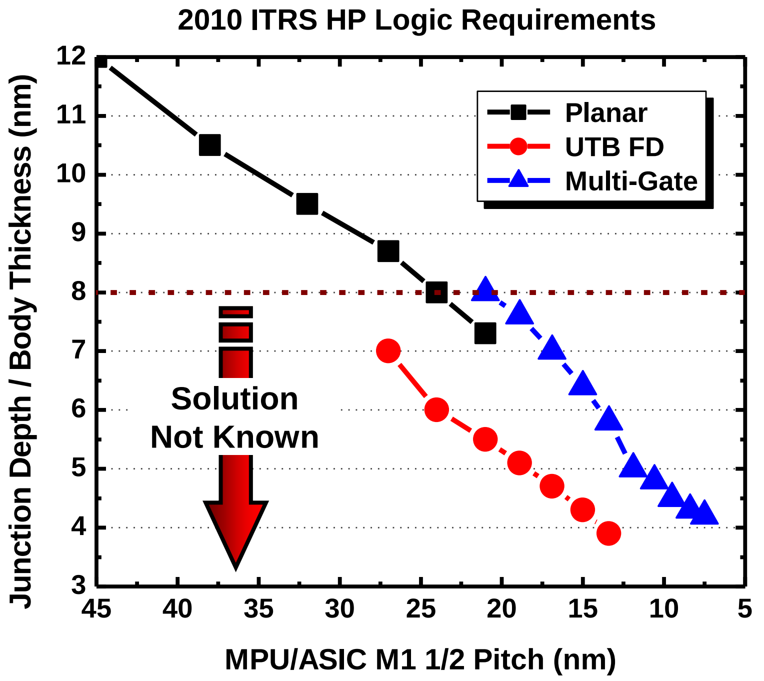
-USJ (Xj~5nm)
-Conformal doping

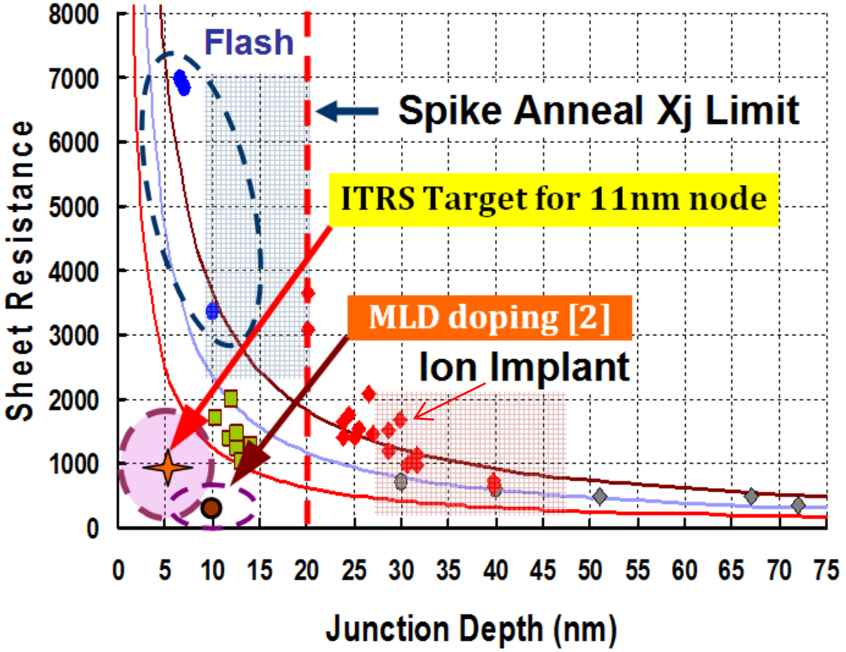
Topography

-Gate/spacer etch
-CMP polish challenge

Junction Scaling Challenges in Advanced Nodes

Enabling junction scaling in advanced nodes beyond 11nm


2010 ITRS HP Logic Requirements

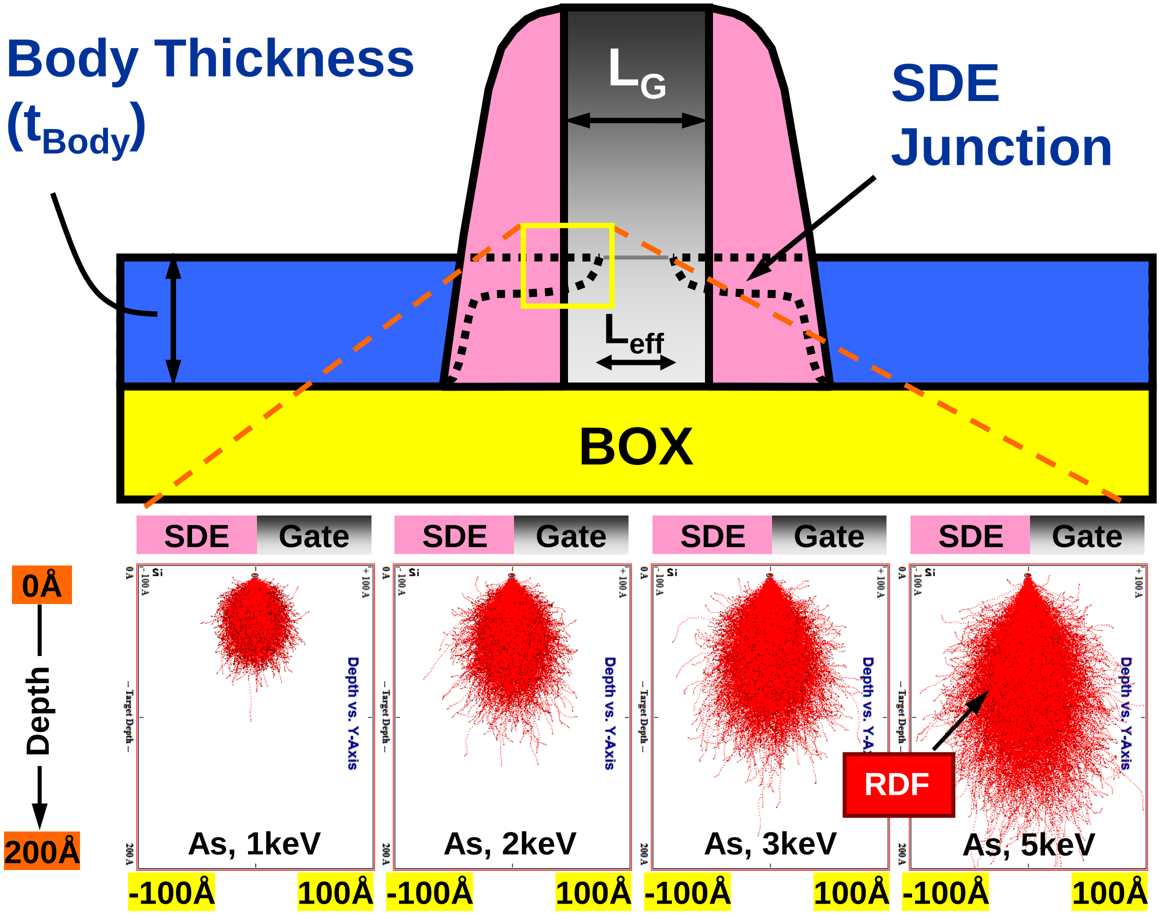


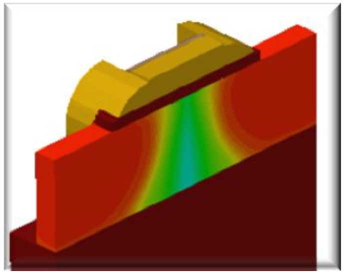
- ITRS roadmap calls for a sub-5nm junction for beyond 14nm node.
- Current beam-implant technology is running out of steam to keep up with this aggressive Xj scaling.
- Monolayer doping technique could be a key enabling technology to extend FinFET scaling beyond 14nm node.

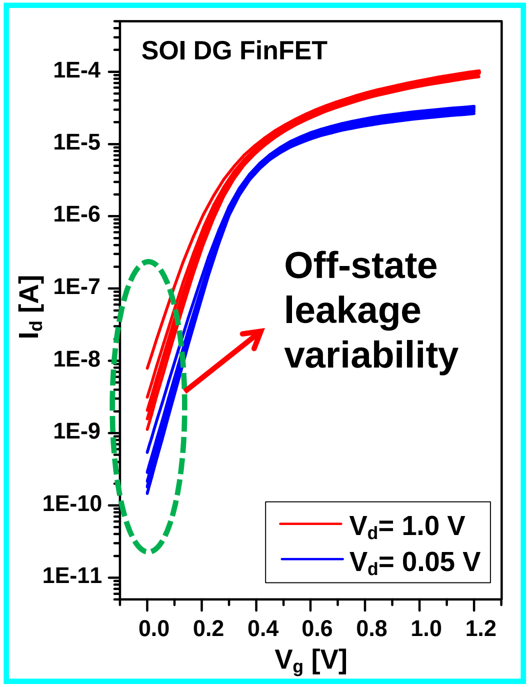
K-W. Ang, et al., IEDM 2011

Random Dopant Fluctuations (RDF) Issue

RDF issue due to ion implantation impedes further junction scaling



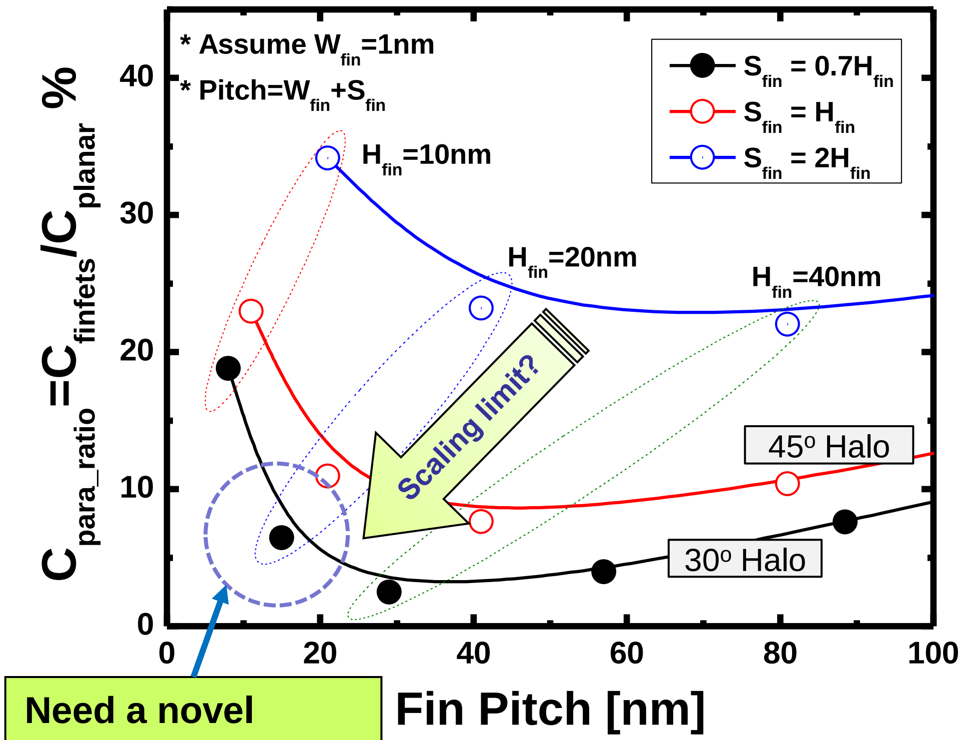




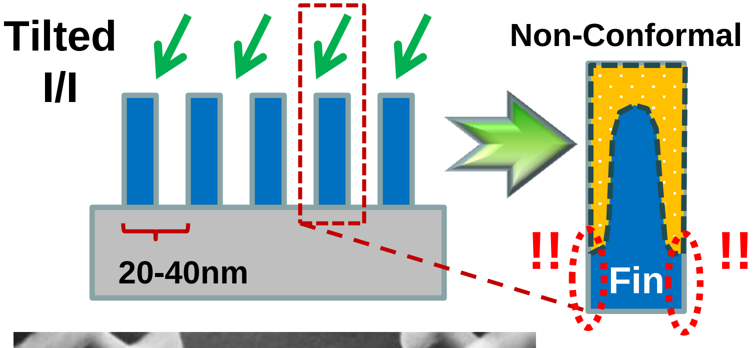
- Severe lateral dopant encroachment will be unmanageable in Lg<20nm
- Alternative doping approach is needed to overcome the RDF challenge.

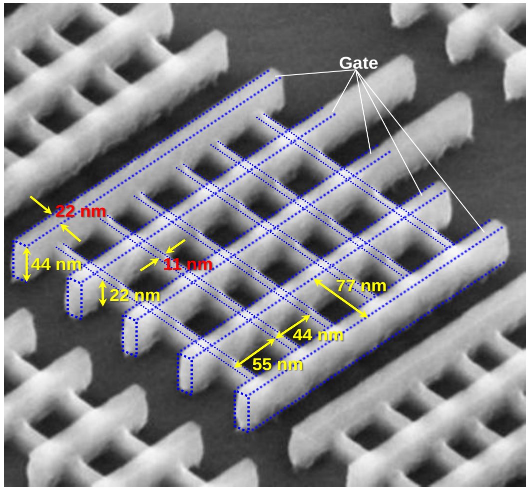
K-W. Ang, et al., IEDM 2011

Alternative Conformal Doping Technique in Dire Need to Support Aggressive Fin Pitch Scaling



Need a novel conformal doping method → MLD





* Intel Announcement, May 2011

High parasitic resistance →Need new conformal doping technique

- **20-60nm Fin pitch is optimum range for C_{para}**
  - Smaller fin pitch cause larger device foot print → Increase C_{con}
  - Larger pitch with higher H_{fin} increase C_{con} & process overhead (Increased overetch for stringer removal) ➔ Optimum H_{fin} : 20~40nm

K-W. Ang, et al., IEDM 2011

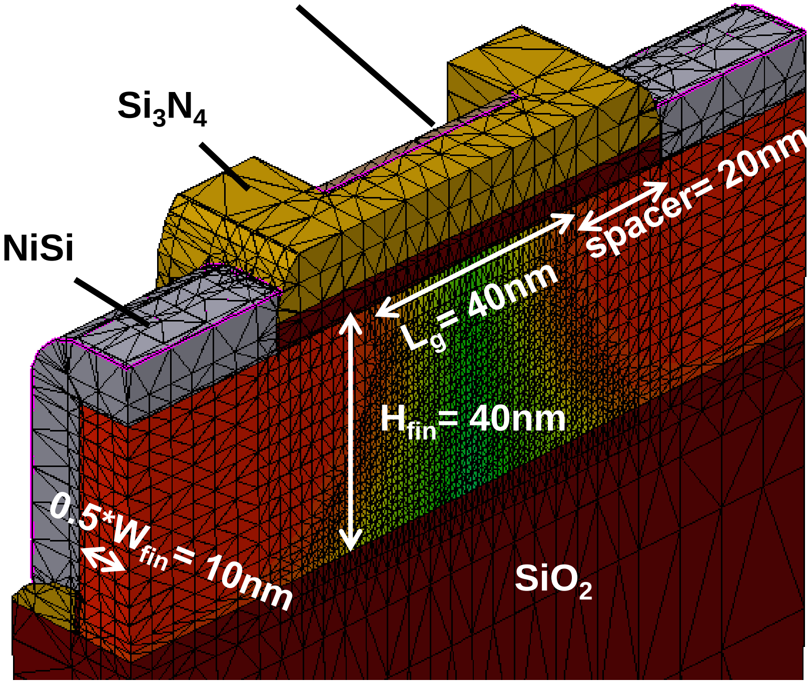
Towards the Limits of Ion Implant

(Ion implant = I/I)

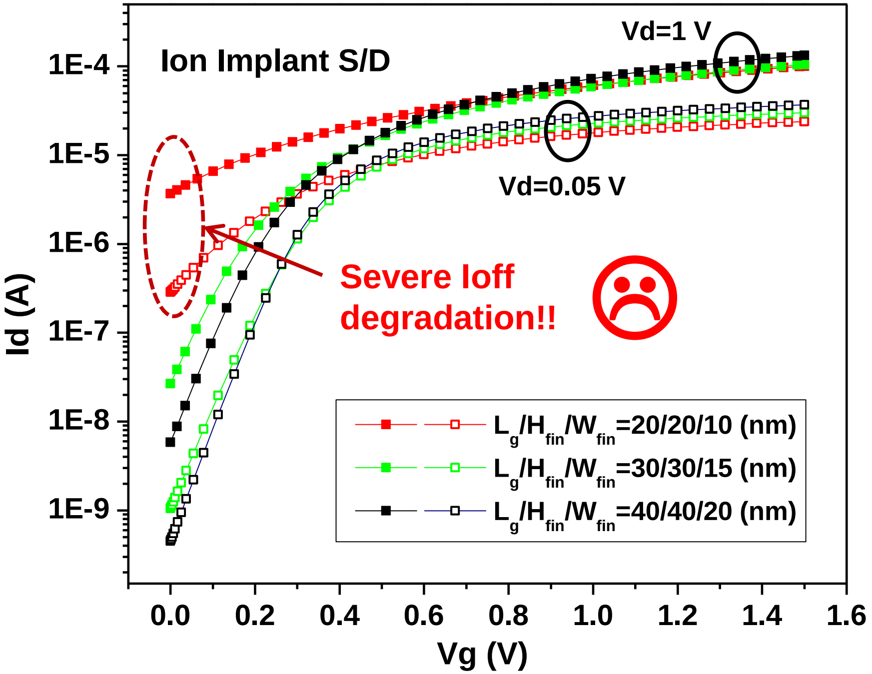
Double-Gate SOI FinFET Structure

- Hard mask nitride
- Fin formation
- SiO_2/HK and TiN/Poly Si
- Offset spacer and S/D implantation
- S/D implantation and spike anneal
- Contact formation

TiN and Poly Si were stripped



[DG SOI FinFET with SiO_2=1 nm, HfO_2=2 nm]

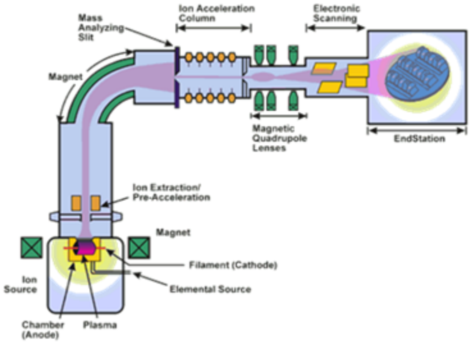
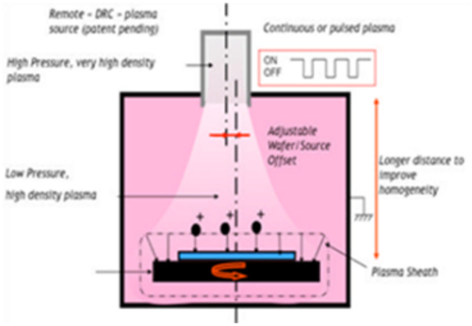
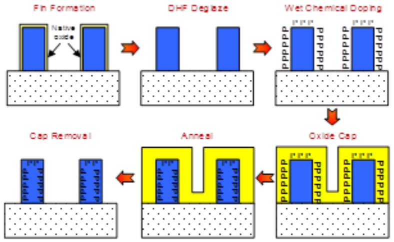


- **What we need to enable further L_g scaling below sub-20 nm?**

1. Excellent lateral diffusion control or more thermal budget → **improves SCE margin**
2. Uniform conformal doping → **reduce parasitic and I_{on} variation from die to die**
3. Highly doped S/D extension → **reduce S/D resistance for high Ion**

K-W. Ang, et al., IEDM 2011

Alternative Non-Planar Doping Technologies

Option	Beam line	Plasma	Mono Layer Doping
			
Conformal Doping	Challenges to achieve conformal doping	Moderate (Better than I/I)	Uniform & Conformal around Fin
FIN Damage	High Damage	Low damage for AsH_3 & B_2H_6.	No Damage (Wet Chemical Doping
Dose	Good doping	Fin-Width, Thermal Budget Dependent	Fin-Width, Thermal Budget Dependent
Results	▪ Fin damage ▪ Junction depth ~30nm	▪ Low damage ▪ Relatively low dopant activation	▪ ZERO damage ▪ USJ ~ sub-10nm ▪ Highly conformal

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- ☐ Monolayer Doping Process Technology
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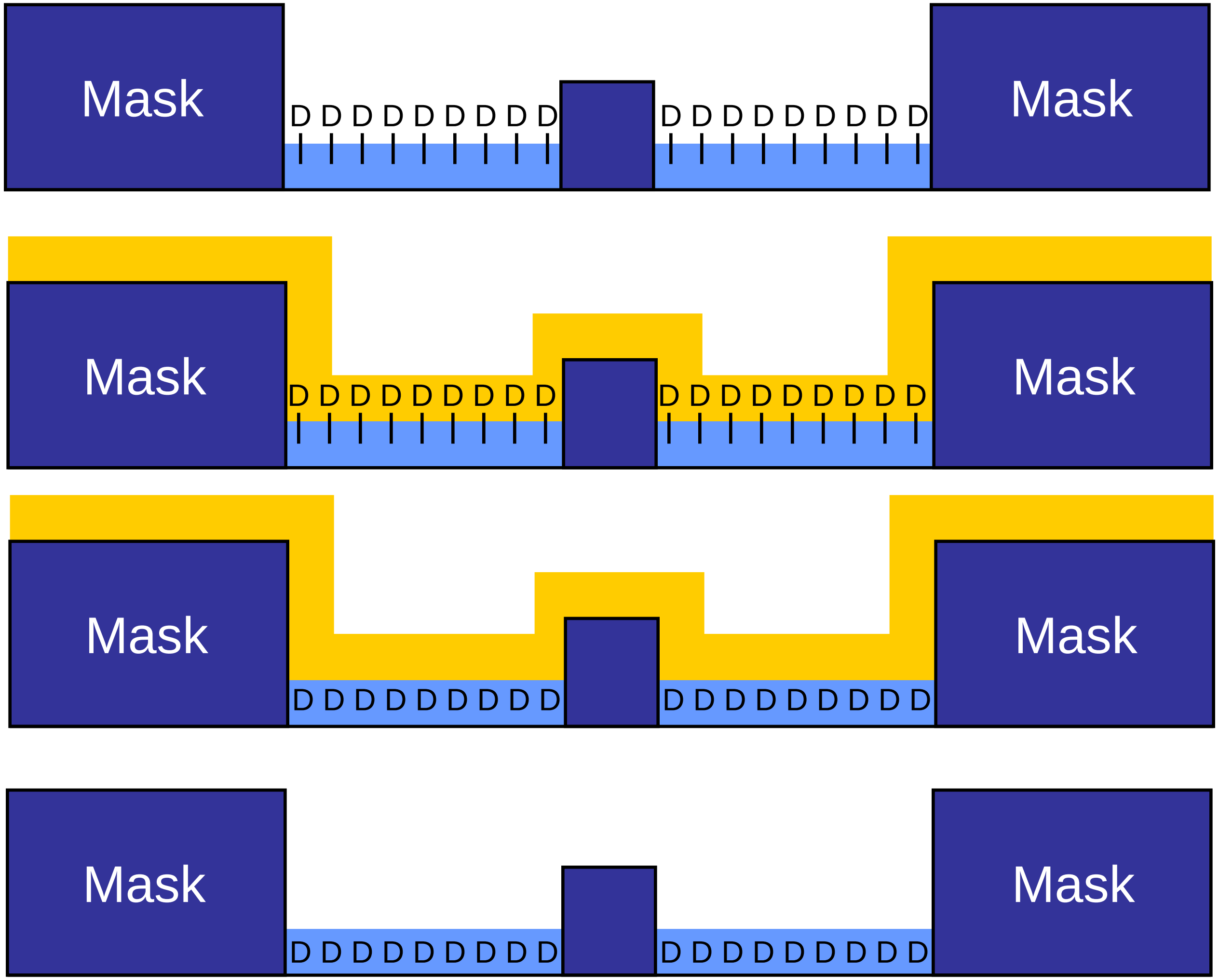
Mono Layer Doping (MLD)

Elegant solution to ultra shallow junction formation

→ excellent uniformity and self-limiting



Wet chemical doping

Cap

Anneal

Cap removal

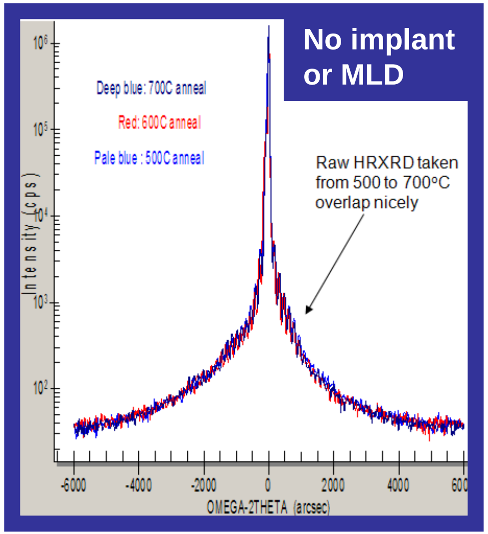
J. Barnett, et al., UCPSS 2010

Benefits of Monolayer Doping

- Sub 10-nm junctions achievable
- No implant damage to substrate
- Excellent method for doping non-planar structures
- Low equipment and processing costs

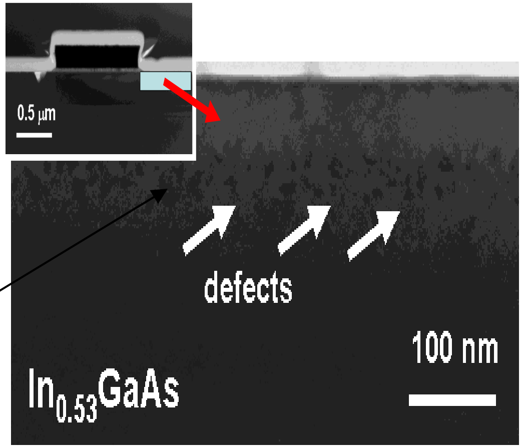
- Applicable to various substrates (Si, SiGe, Ge, III-V)
- Long roadmap envisioned for MLD

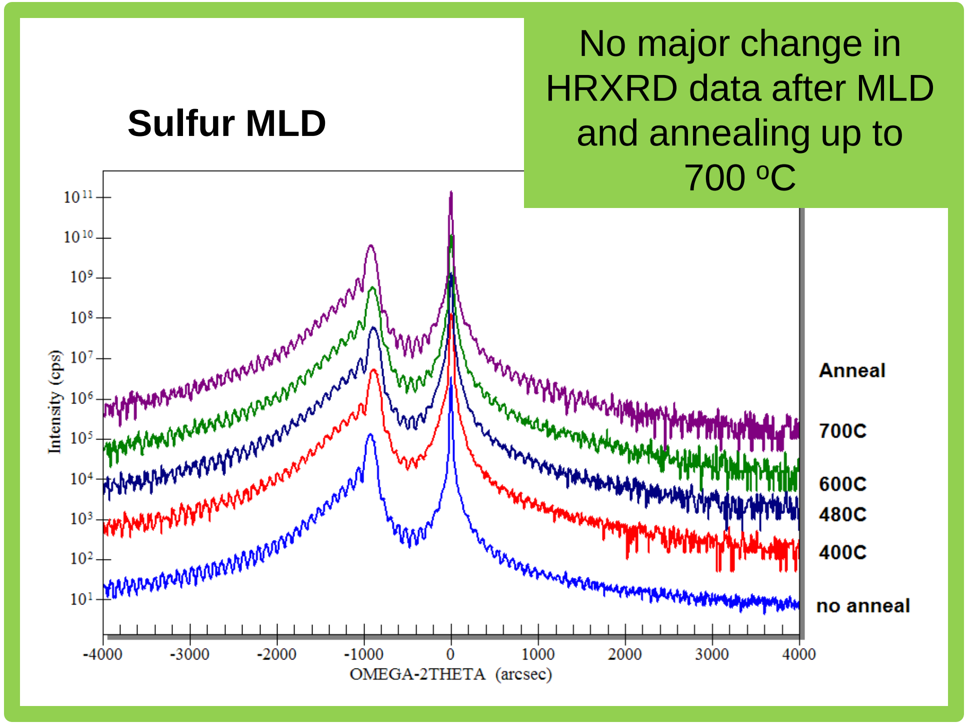
MLD Advantage over Ion implantation


No implant or MLD

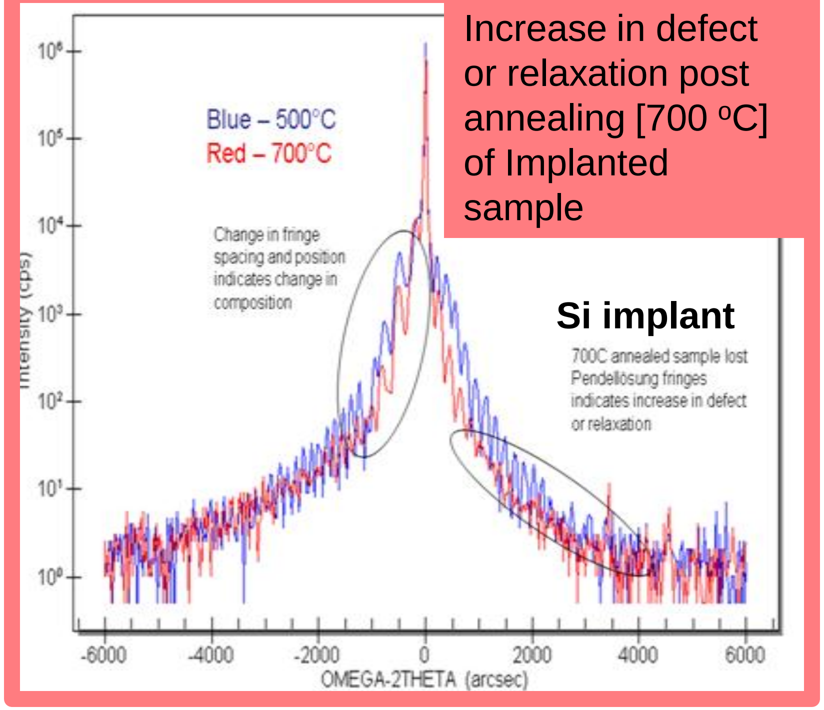
Raw HRXRD taken from 500 to 700ºC overlap nicely

High resolution X-Ray Diffraction on $In_{0.53}GaAs$/ InP indicates lattice quality deteriorates for implanted sample but not for non-implanted or MLD sample




Sulfur MLD

No major change in HRXRD data after MLD and annealing up to 700 ºC


Increase in defect or relaxation post annealing [700 ºC] of Implanted sample

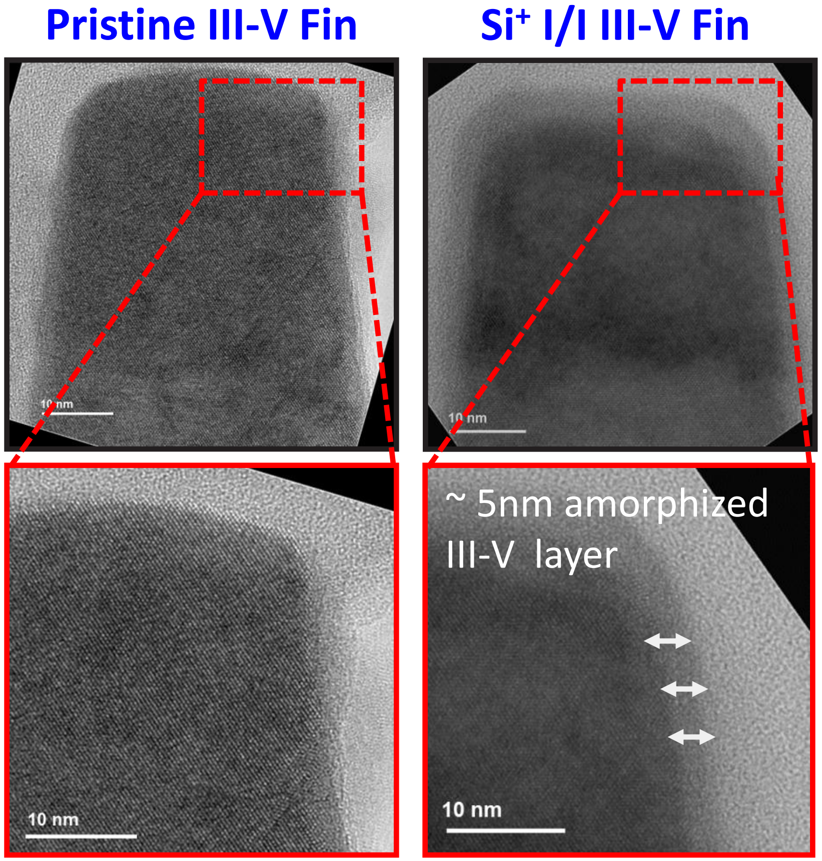
Si implant

Change in fringe spacing and position indicates change in composition

700C annealed sample lost Pendellösung fringes indicates increase in defect or relaxation

J. Barnett, et al., UCPSS 2010

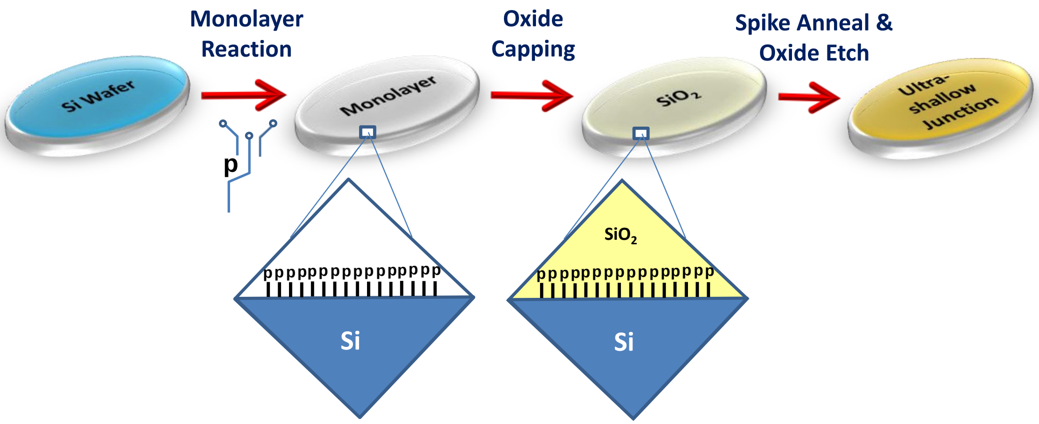
Ion implantation impedes iii-V fin progress

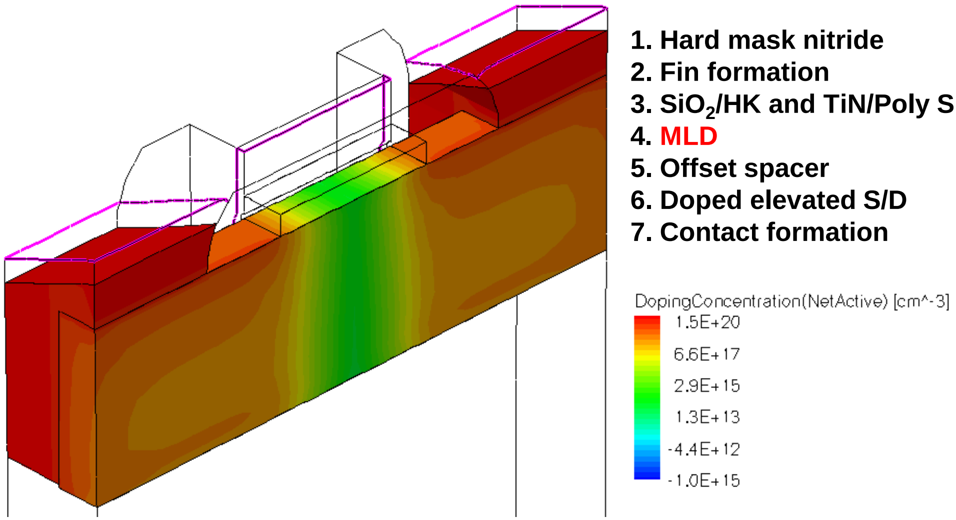


- I/I is expected to completely amorphize a III-V Fin when we scale **W_{FIN} to ~ 10nm.** Hence, no/low damage doping techniques will be critical for scaled Fins.
- New low damage 3D compatible doping method (MLD) required for next generation

(Ion implant = I/I)

MonoLayer Doping Enables USJ &Abrupt Junction

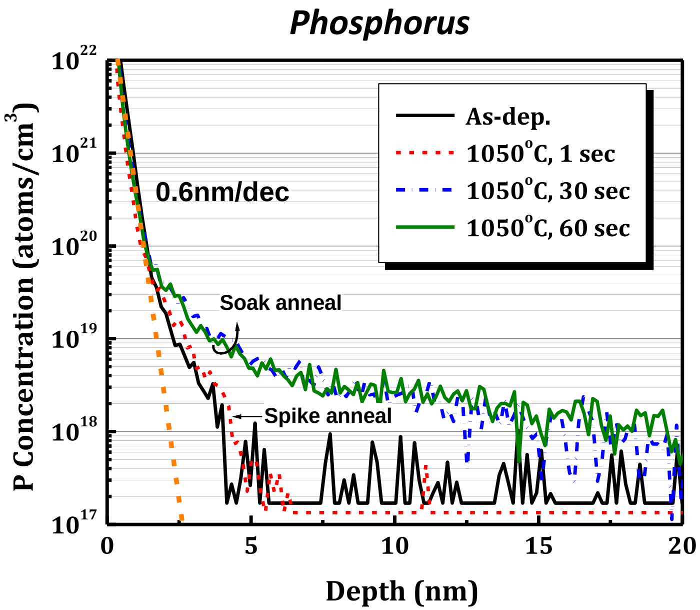


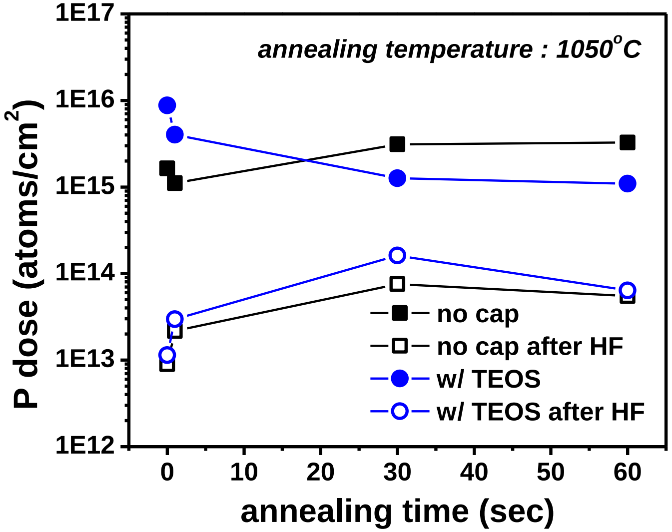


1. Hard mask nitride
2. Fin formation
3. SiO_2/HK and TiN/Poly Si
4. MLD
5. Offset spacer
6. Doped elevated S/D
7. Contact formation

✓ **Excellent lateral diffusion control**

✓ **Conformal doping around high aspect ratio fin**

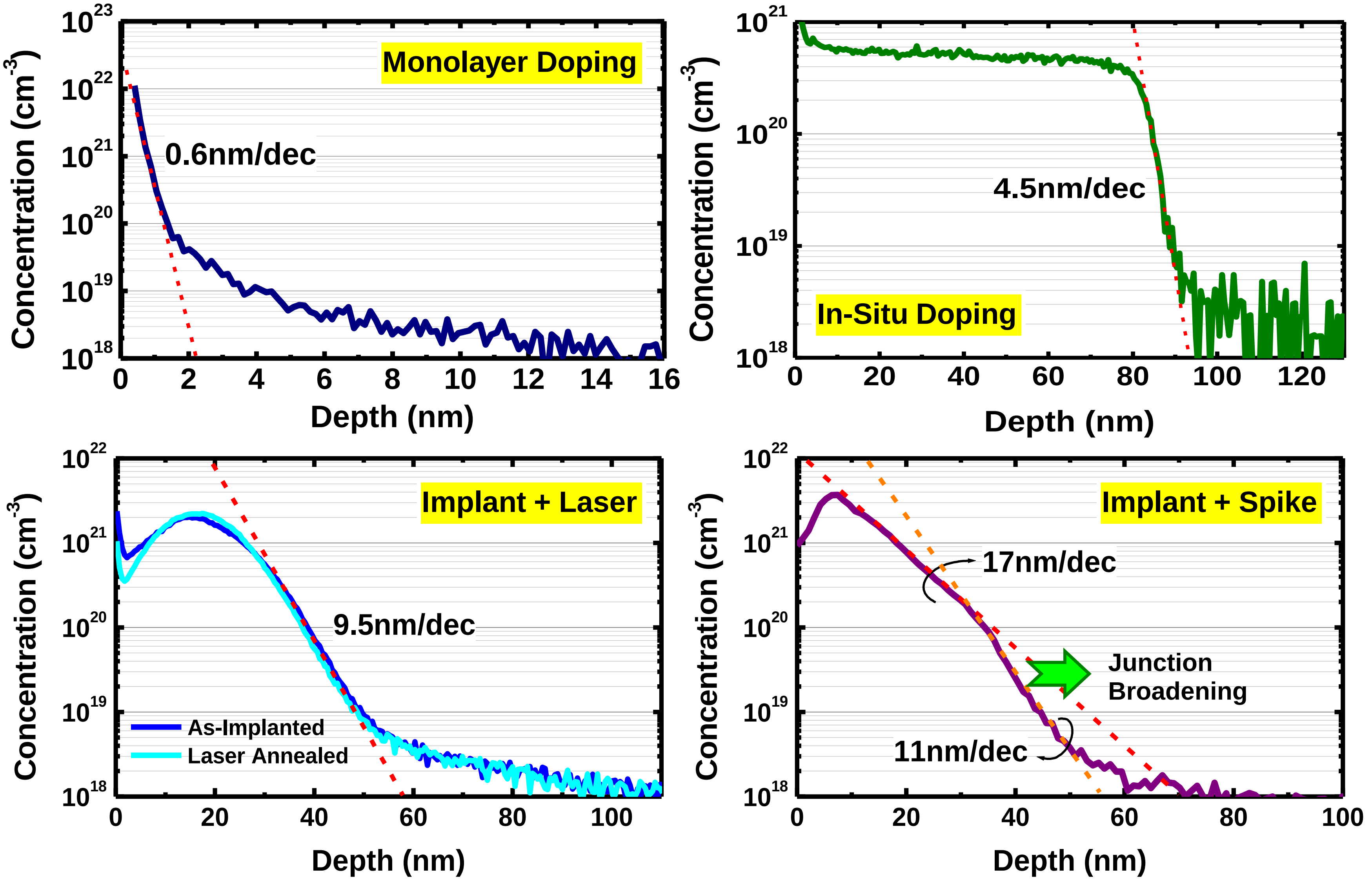




K-W. Ang, et al., IEDM 2011

A Comparison of Junction Abruptness

MLD doping shows steepest junction

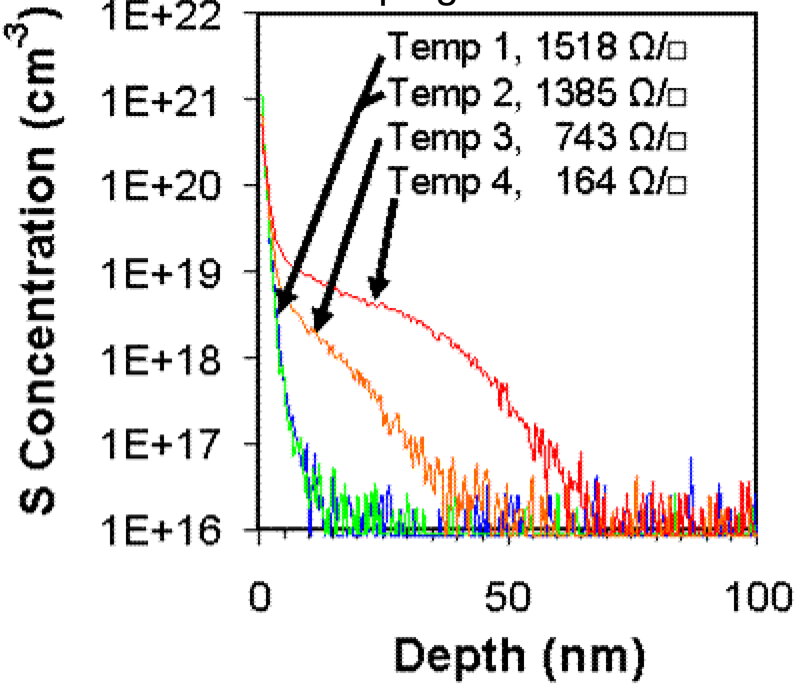


K-W. Ang, et al., IEDM 2011

Effect of RTA Temperature on Sulfur doping using MLD

- < 500 ˚C, 30 s
  - X_j < 3nm*, R_{sh} > 1300 Ω/sq
  - Doping profile ~ 1 nm/dec
- > 500 ˚C, 30 s
  - X_j = 9 nm*, R_{sh} = 164 Ω/sq
  - Long diffusion tail

S doping to InGaAs

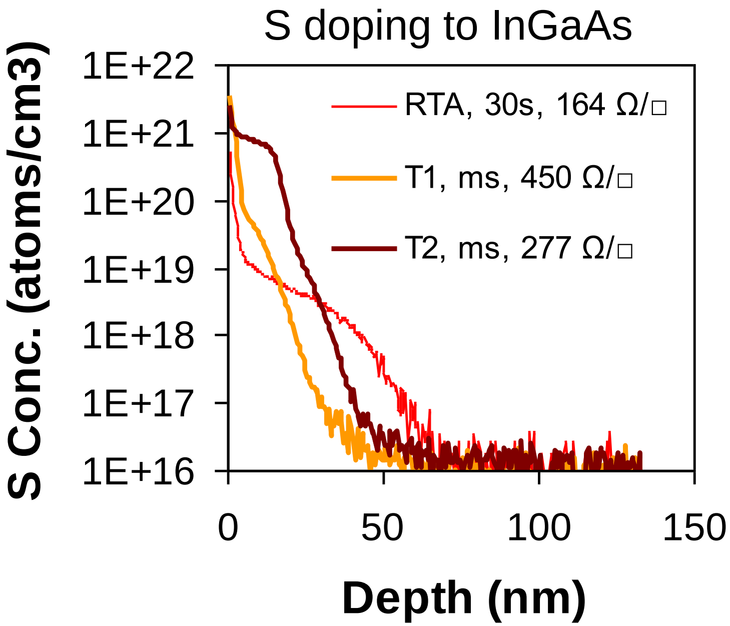


N_d and X_j increase with temperature

J. Barnett, et al., UCPSS 2010

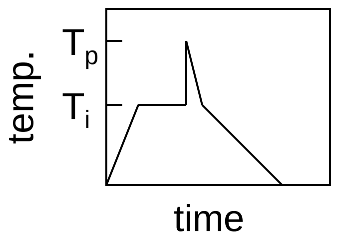
Effect of ms-Flash Anneal for Sulfur doping using MLD

Sample	R_{sh}*	μ*	n*
	Ω/sq	cm^2/Vs	$x10^{12}$ cm^{-2}
$Temp_1$	450	3200	4.3
$Temp_2$	277	1460	15
RTA, 30s	164	2682	14


S doping to InGaAs

Ms-flash has higher near surface concentration, but not increased activation, further optimization necessary.

Ms- flash profile

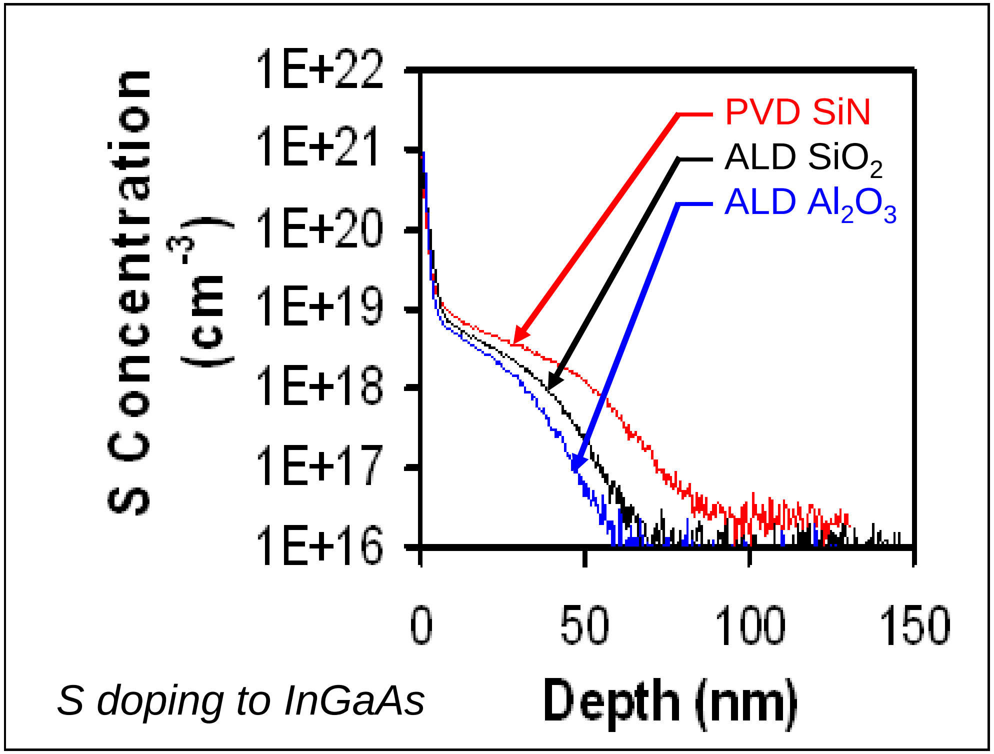


* VdP Hall data. ** Estimated T_p

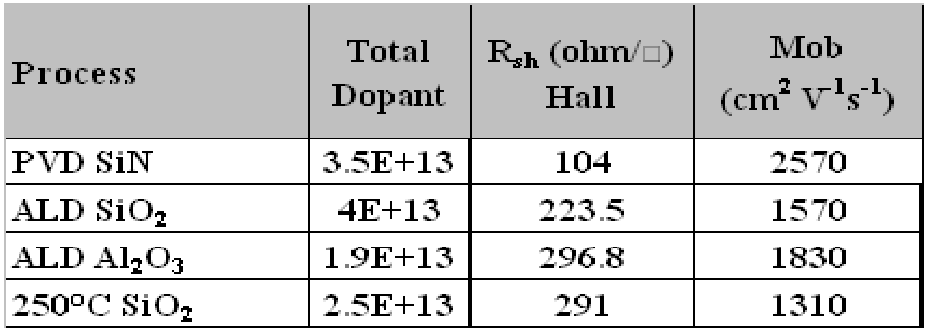
J. Barnett, et al., UCPSS 2010

Effect of Capping Layer for Sulfur doping using MLD

- Cap type influences S incorporation
- Attributable to temperature of deposition
- S desorbs at temps ≥ 250 °C



S doping to InGaAs

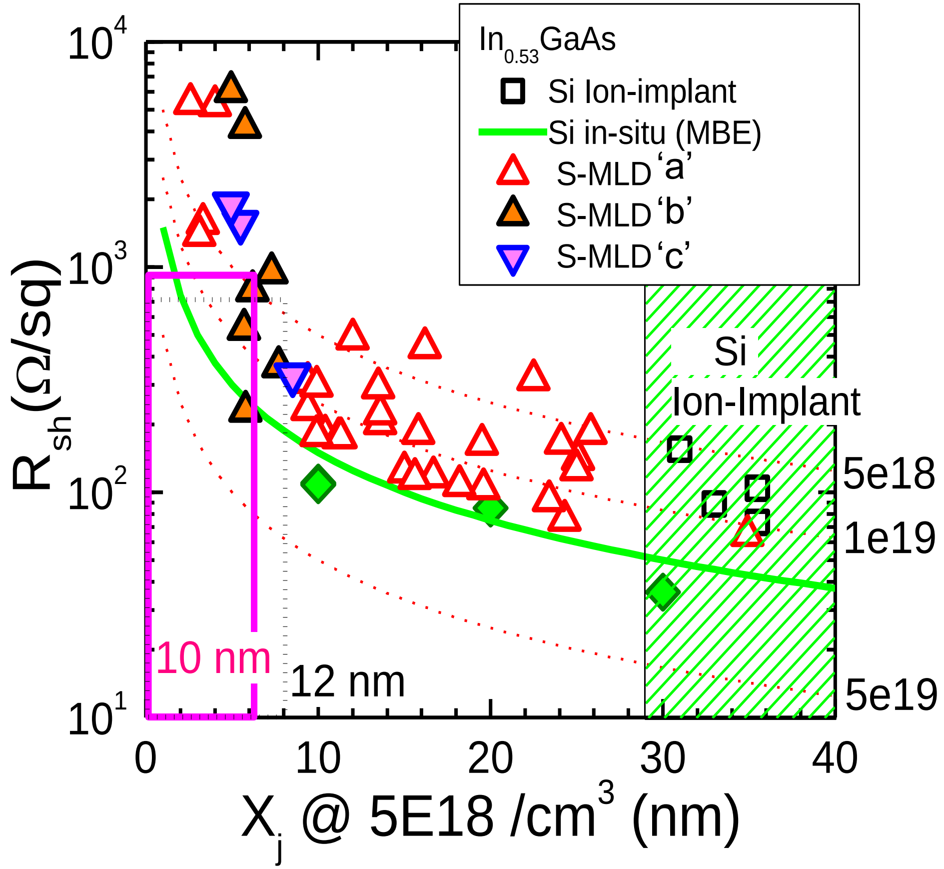


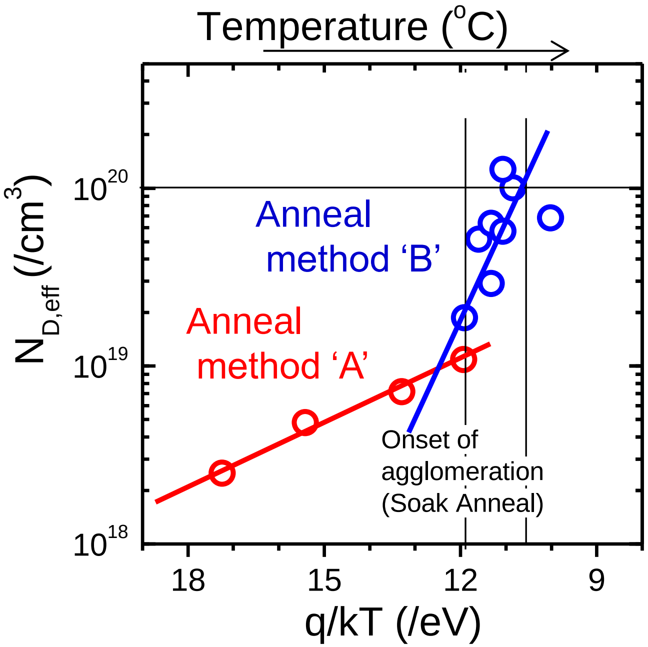
Process	Total Dopant	R$_{sh}$ (ohm/□) Hall	Mob (cm^2 V^{-1}s^{-1})
PVD SiN	3.5E+13	104	2570
ALD SiO$_2$	4E+13	223.5	1570
ALD Al$_2$O$_3$	1.9E+13	296.8	1830
250°C SiO$_2$	2.5E+13	291	1310

J. Barnett, et al., UCPSS 2010

Advanced Junction Solutions

~ *S-MLD meets ITRS 10nm node specification*

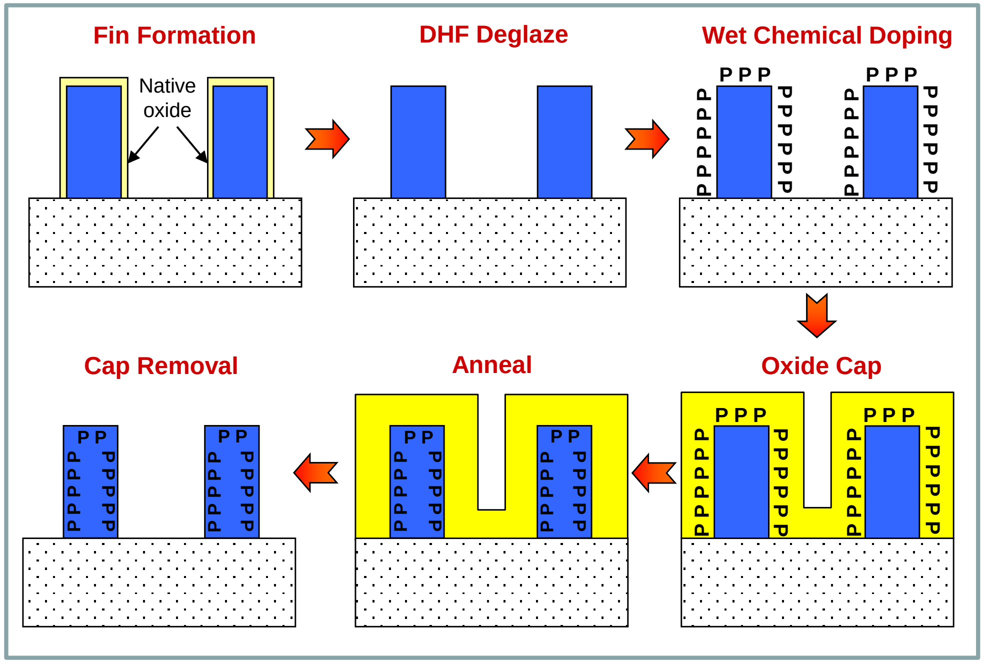


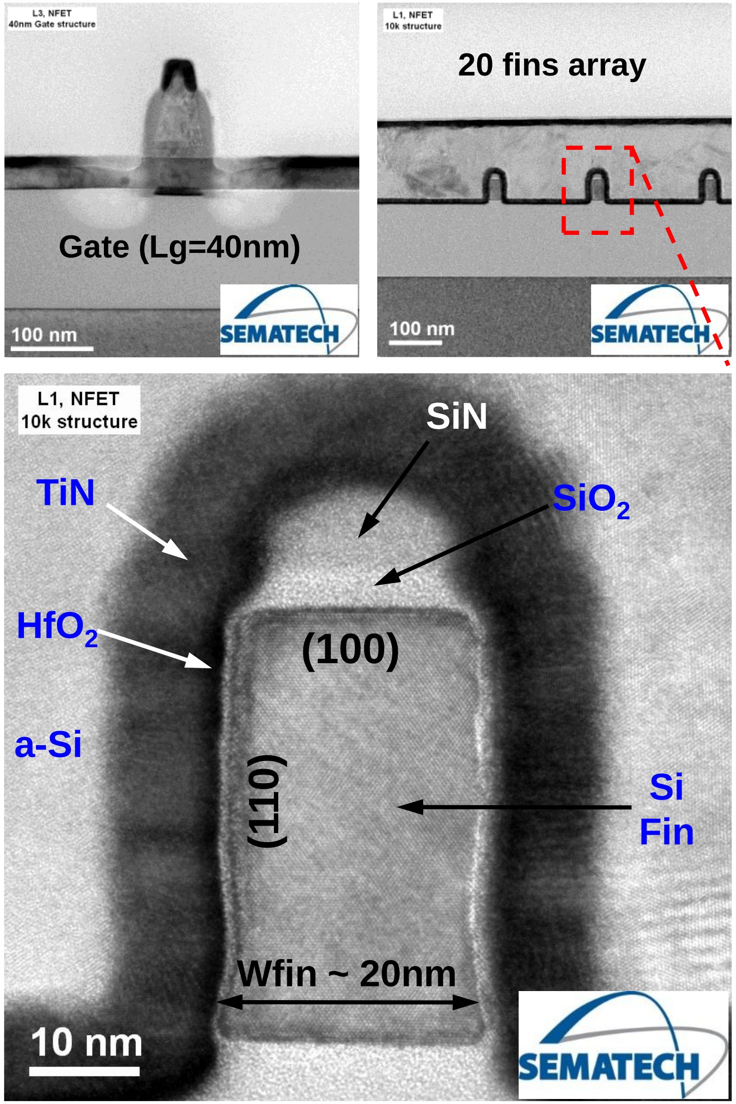


S-MLD process is proven to be able to meet 10nm (2021) technology node specification for S/D extension. Flash anneal can activate up to 1e20/cm^3 of S in InGaAs.

Molecular Monolayer Doping for 3D:

Ultra Shallow Junction, Defect-Free & Conformal Doping with MLD

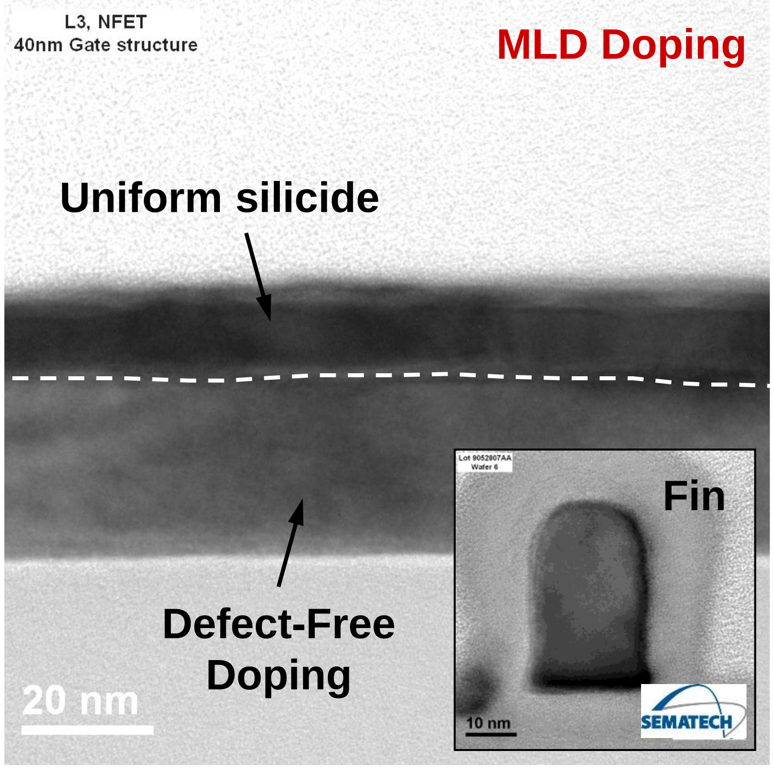

Fin Formation
DHF Deglaze
Wet Chemical Doping
Oxide Cap
Anneal
Cap Removal

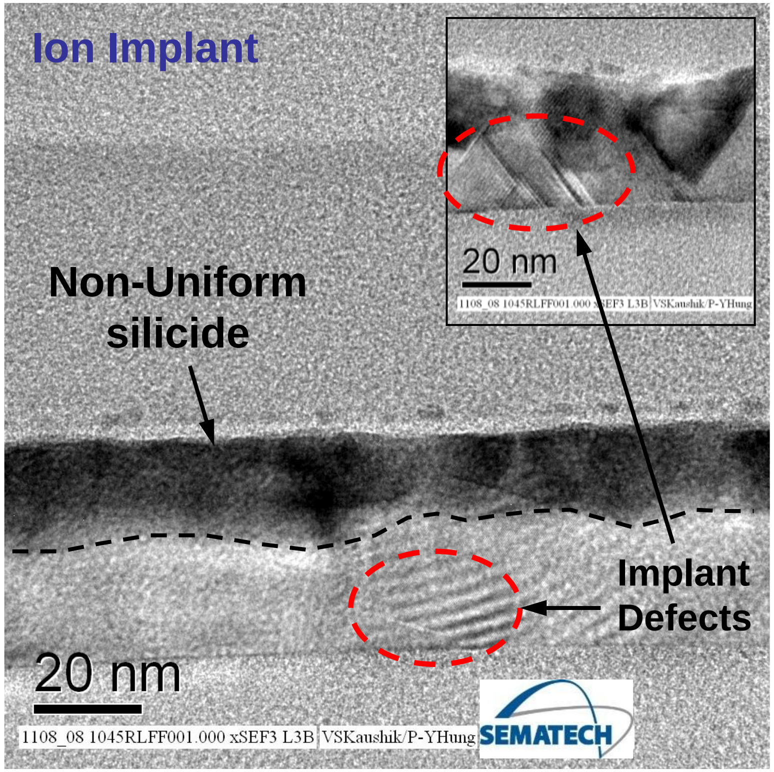


- **Highlights of MLD Doping**
  1. **Ultra-Shallow Junction:** Xj < 10nm.
  2. **Defects-Free (No implant damage):** Low leakage → Good for LSTP applications
  3. **Conformal Doping:** Best known method for doping non-planar structures (Si, SiGe, Ge, III-V)

K-W. Ang, et al., IEDM 2011

Silicidation on MLD Fin vs I/I Fin



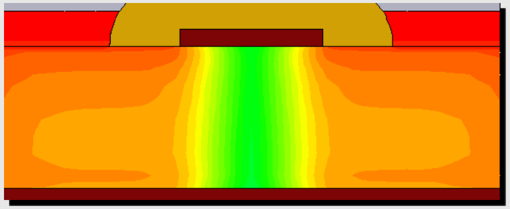
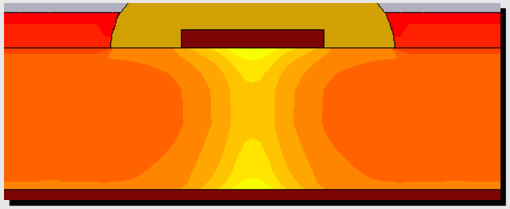
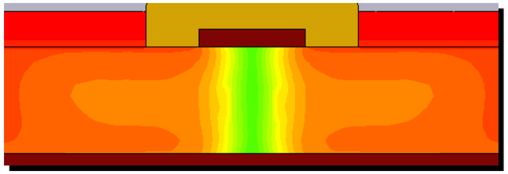
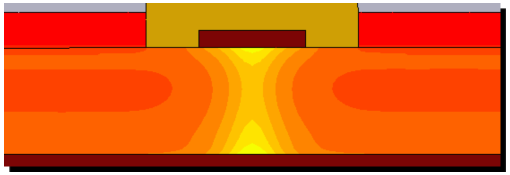
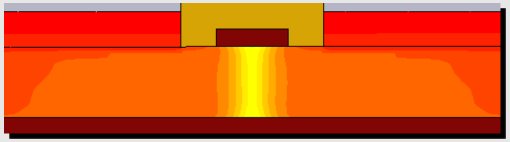
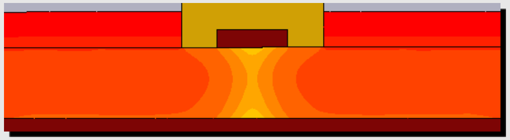


- **Uniform silicide formation and defect-free doping**
  - MLD approach shows excellent silicide uniformity and zero Fin damage (important for lowering Fin resistance)
  - I/I approach is inferior due to severe implant defects & non-uniform silicide

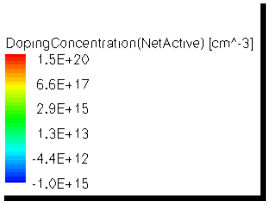
K-W. Ang, et al., IEDM 2011

MLD Shows Better Dopant Profile Control

- **MLD vs. I/I extension for phosphorus doping**
  - Dose of each structure are chosen when the peak doping concentration is almost same at L_g=40 nm
  - The same dose were applied regardless of L_g at the same structure
  - Even though using longer annealing time, MLD show excellent short channel margin than I/I extension. It can be further improved when we use the Arsenic MLD

	MLD	**I/I extension**
$L_g/H_{fin}/W_{fin}$ (40/40/20 nm)		
$L_g/H_{fin}/W_{fin}$ (30/30/15 nm)		
$L_g/H_{fin}/W_{fin}$ (20/20/10 nm)		
Anneal condition	**1050 C/ 4.5 sec**	**1050 C/ 0.7 sec**
Thermal budget	☺	☹
Lateral diffusion	☺	☹
Doping uniformity	☺	☹

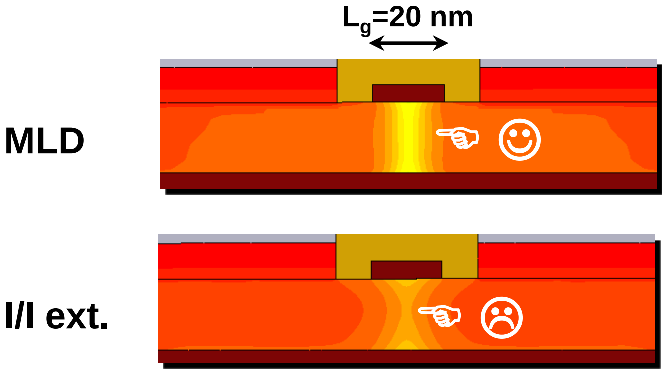
1. **Hard mask nitride**
2. **Fin formation**
3. **SiO_2/HK and TiN/Poly Si**
4. **MLD vs I/I extension**
5. **Offset spacer**
6. **Doped elevated S/D**
7. **Contact formation**

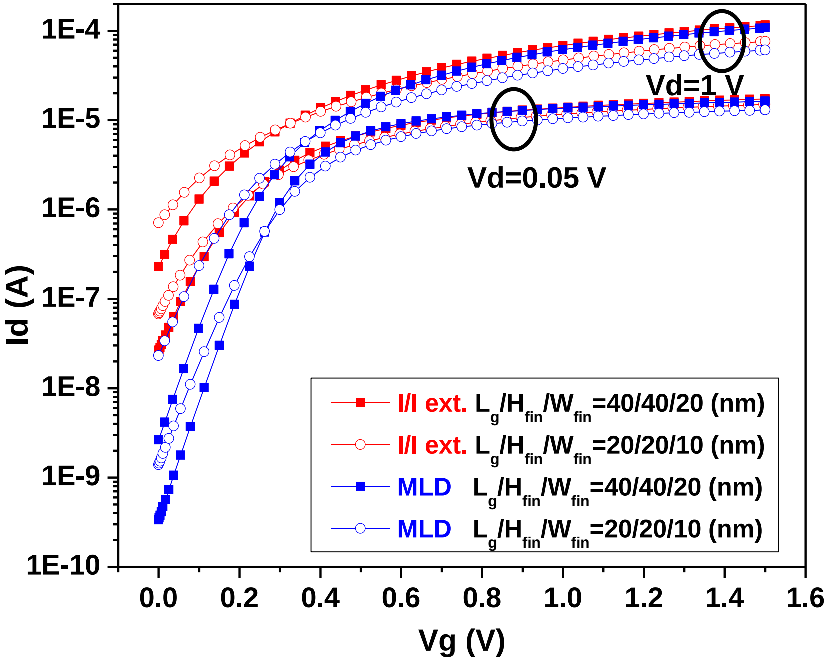


K-W. Ang, et al., IEDM 2011

MLD Enables Aggressive Lg Scaling

✓ **Id-Vg comprison bet. MLD and I/I extension**
- MLD show shows excellent short channel margin without large I_{on} drop





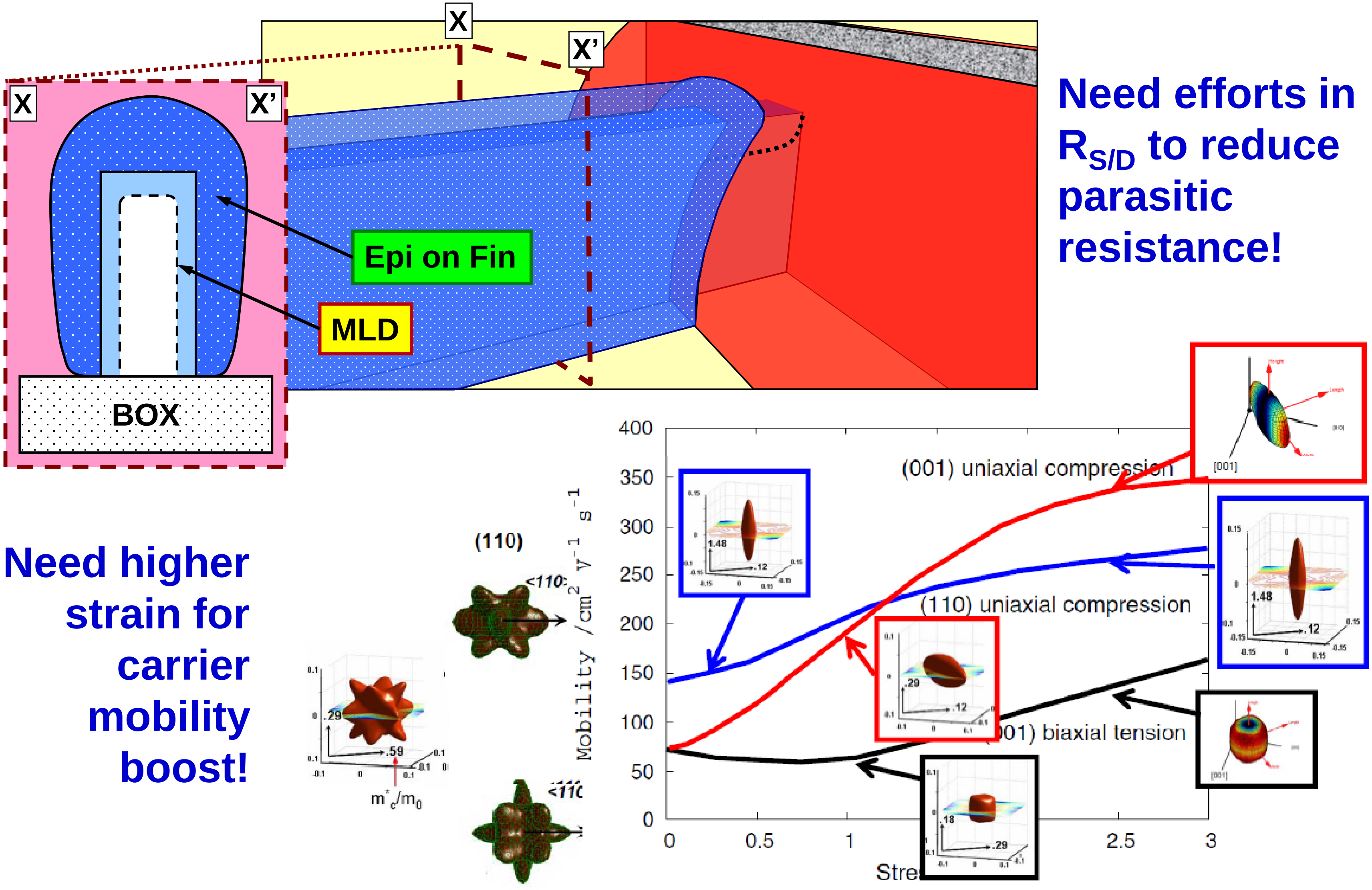
🟩 better

Geometry	$L_g/H_{fin}/W_{fin}$=40/40/20 (nm)		$L_g/H_{fin}/W_{fin}$=30/30/15 (nm)		$L_g/H_{fin}/W_{fin}$=20/20/10 (nm)	
Process	**MLD**	**I/I ext.**	**MLD**	**I/I ext.**	**MLD**	**I/I ext.**
I_{on}(Vg=Vd=1V) (A)	6.16E-5	6.84E-5	5.03E-5	5.71E-5	3.77E-5	4.73E-5
I_{off}(Vg=0V,Vd=1V) (A)	2.65E-9	2.29E-7	4.94E-9	2.22E-7	2.32E-8	7.1E-7
DIBL(@Id=1E-7) (mV/V)	73	> 150	84	> 150	116	> 150
SS(@Vd=0.05 V) (mV/dec)	82	166	88	156	105	217

K-W. Ang, et al., IEDM 2011

Need More Efforts into $R_{S/D}$ & Strain for fins

FinFET/NW FET Enhances Scalability but High R_{SD} Limits Performance…



Need efforts in $R_{S/D}$ to reduce parasitic resistance!

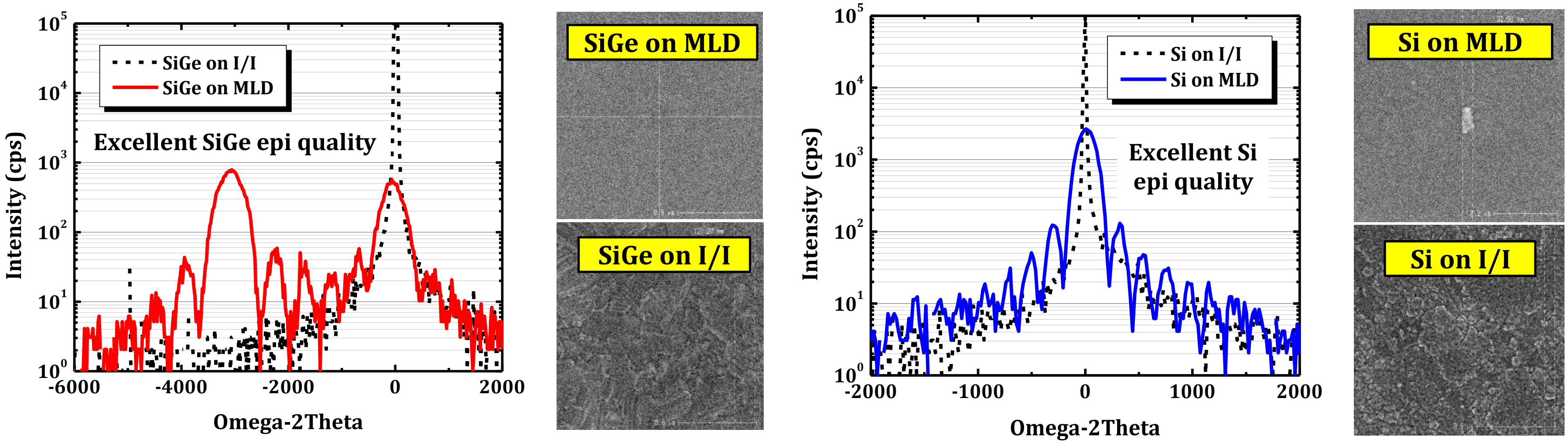
Need higher strain for carrier mobility boost!

K-W. Ang, et al., IEDM 2011

Molecular Monolayer Doping (MLD) Process

Damage-free surface improves hetero-epitaxy quality→ MLD is ‘epi-friendly’

Dual Epi (SiGe & Si Elevated S/D)



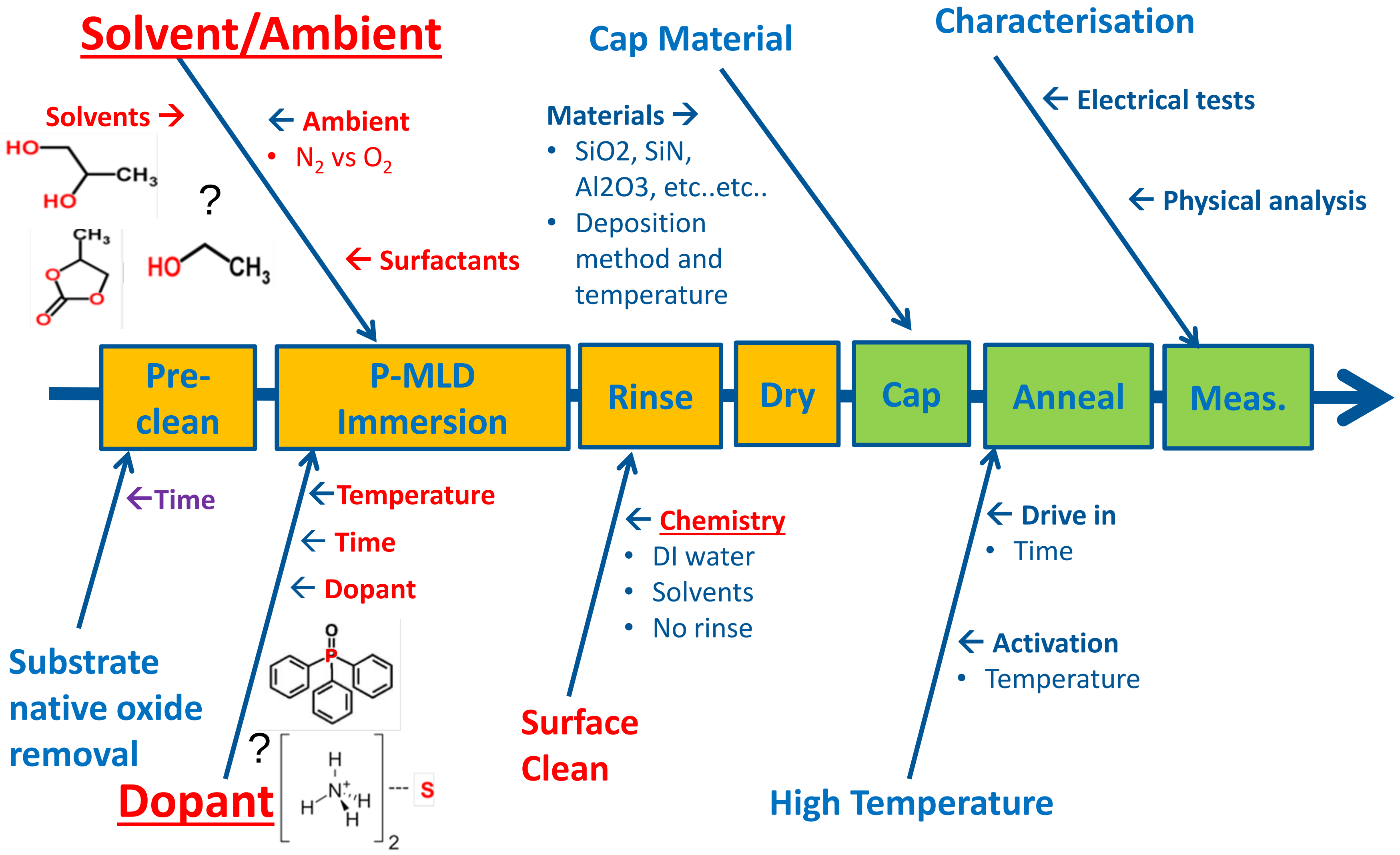
- Due to a damage-free doping, pseudomorphic SiGe and Si epitaxy on MLD substrate with excellent single crystalline quality were demonstrated, coupled with smooth surfaces.

- When grown on an I/I substrate, the pendellosung fringes of the epitaxy films broaden and smear because of severe crystal defects, often accompanied by strain relaxation.

K-W. Ang, et al., IEDM 2011

Key Process Parameters for MLD

- Purpose: MLD Dopant/ Solvent Screening & Optimization → lots of space for the Chemist!



MLD Prospect & Scalability Beyond 20nm Node

- **DG SOI FinFET simulation summary**

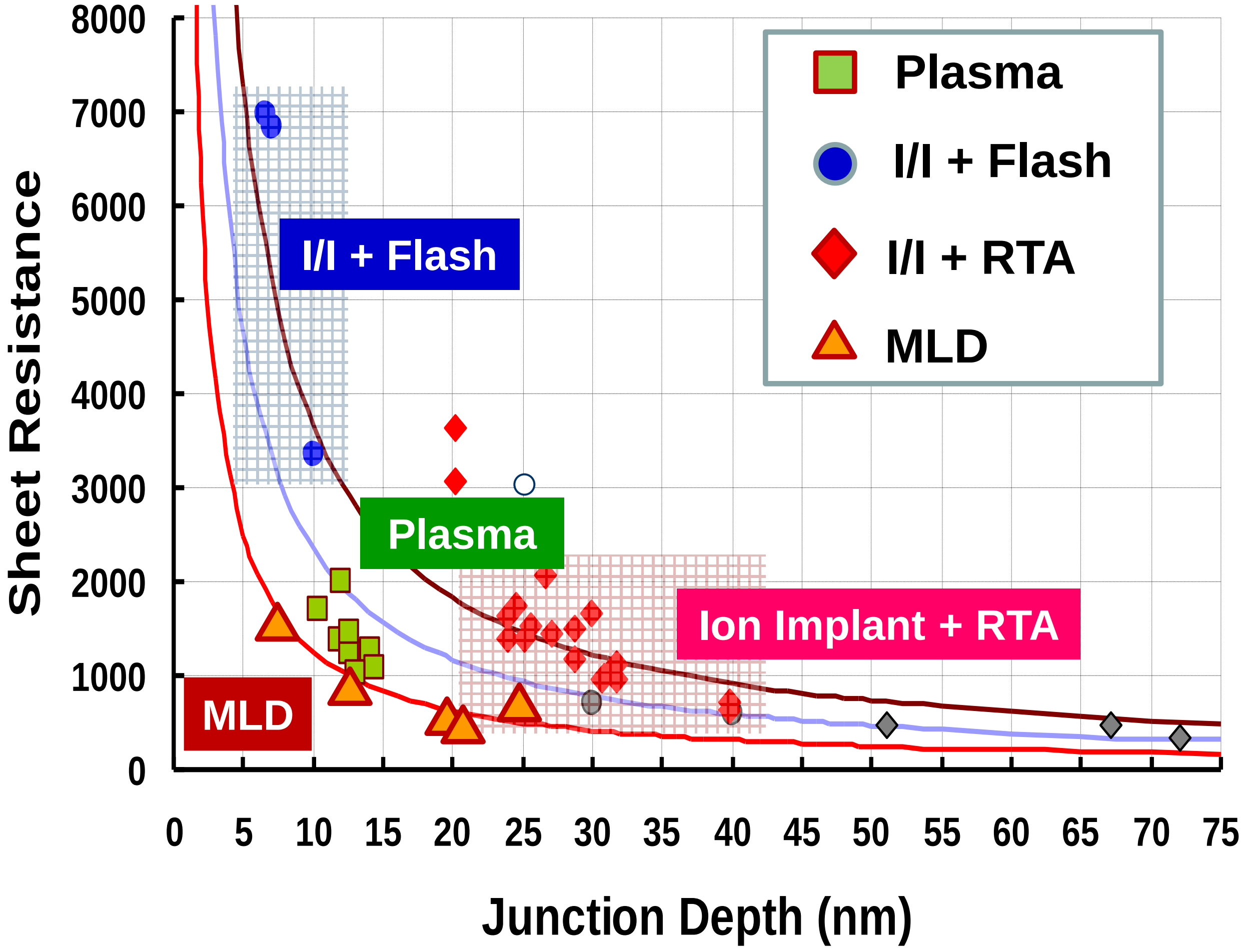
🟩 Good 🟨 Can be improved 🟥 Danger

	L_g= 40nm	L_g= 30nm	L_g= 20nm	L_g= 10nm
I/I S/D + NiSi	🟩 - Relatively high I_{on} - Spike annealing	🟨 - Difficult to control overlap	🟥 - Severe lateral diffusion - Low thermal budget - Dopant variability	🟥 - No short channel margin
		[Requirement] - implant (dose, energy) & annealing optimization		
I/I ext + elevated S/D	🟩	🟩 - More thermal buget than I/I S/D	🟨 - Poor short channel margin - Poor dopant variability than MLD	🟥 - No short channel margin
	[Requirement] - I_{on} slightly bigger than MLD, but lower than I/I S/D		[Requirement] - Tri-gate structure - Laser annealing	
MLD + elevated S/D	🟩	🟩	🟩 - Excellent lateral diffusion control - Conformal doping - Low dopant variability	🟨 - Ion performance - Short channel margin
	[Requirement] - Increasing MLD doping up to 5E19 cm^{-3} for large I_{on} - Process test with various dopants (As, Sb, B..)			[Requirement] - Tri-gate or GAA structure - S/D opt. to increase I_{on}

K-W. Ang, et al., IEDM 2011

Rs vs Ultra-Shallow Junction Benchmarking

Comparison of MLD, Plasma and Beamline Methods



- MLD doping shows promise for junction scaling below sub-10nm Xj.

Summary

New materials and new architectures require new doping techniques

- FinFETS - Shallow conformal doping is required!
- III-V Materials – Shallow non-damaging doping is required!

- **Achieved USJ (Xj<10nm), defect-free and conformal doping around high aspect ratio Fin structure with monolayer doping (MLD) process.**
- **Damage free monolayer doping enables the formation of smoother silicide for reduced parasitic resistance in narrow fin.**
- **MLD shows improved epitaxy quality (SiGe & Si) over traditional implant technique → Good for strain retention.**
- **MLD holds great promise for scaling with fin and iii-v beyond sub-10nm regime while maintaining good SCE.**