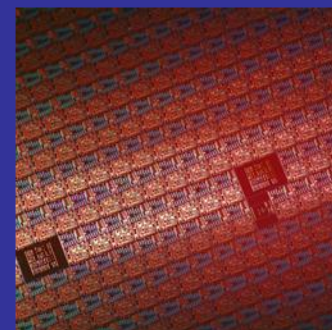
Accelerating the next technology revolution

More Moore or More than Moore?



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Moore's Law

32B in 2020

Curve shows transistor count on integrated circuits doubling every two years

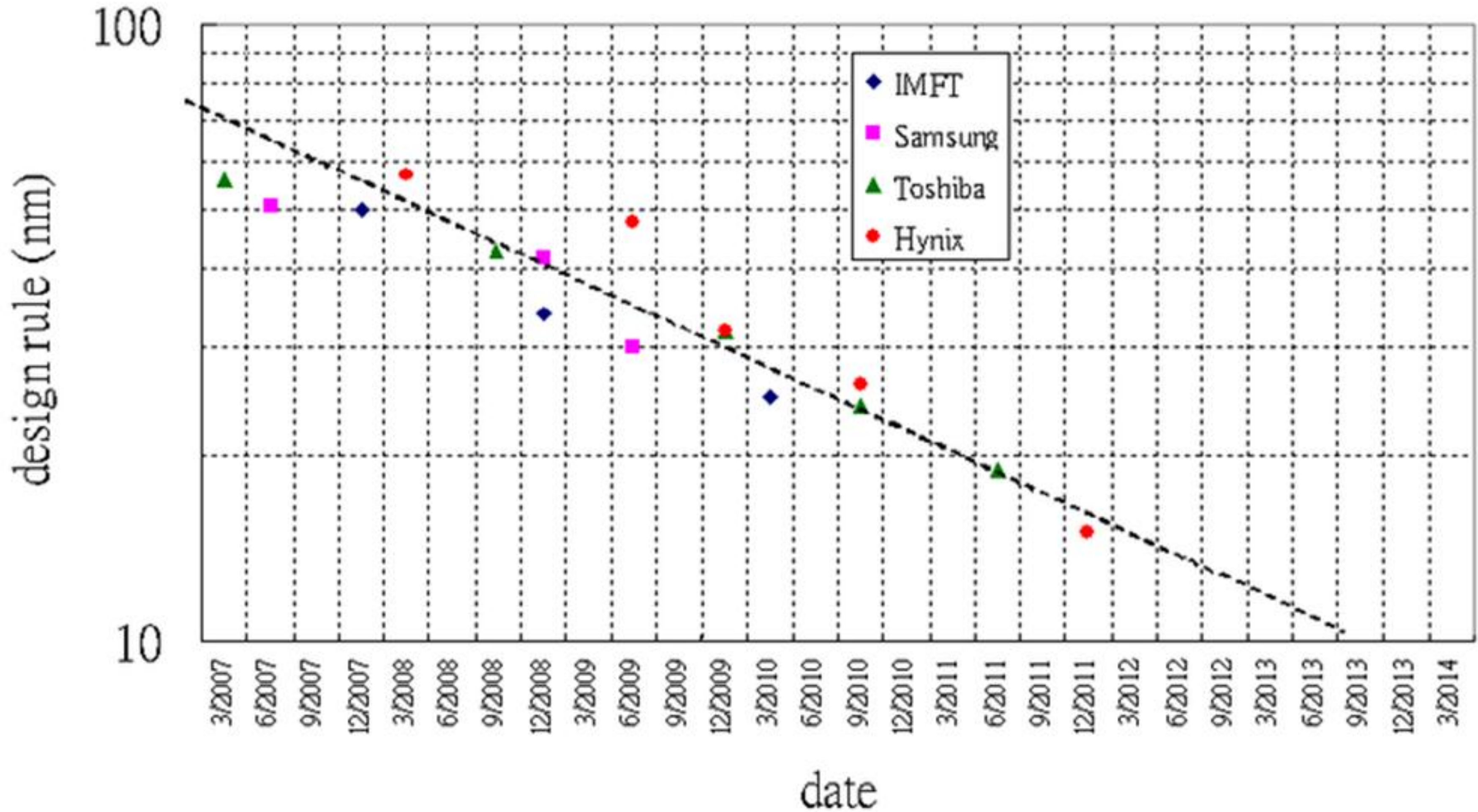
Transistor count

2,600,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300

1971 1980 1990 2000 2011

Date of introduction

NAND flash memory trend allows doubling of components manufactured in the same wafer area in less than 18 months.



Technology Trends

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PC (1990s) → Internet (2000s) → Smart Computing & Connectivity (>2010)

PC | Internet | Smart

1990s | **2000s** | **2010+**

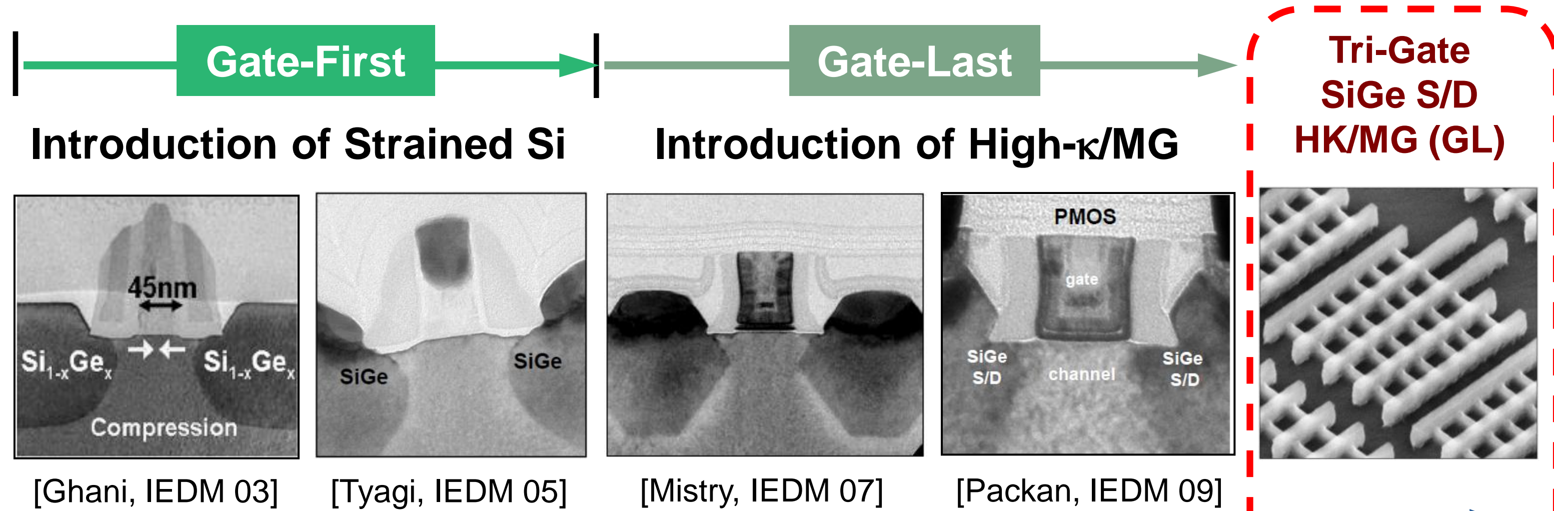
(2011 GSA Forum, Nvidia, 2011 KSIA, Dongbu)

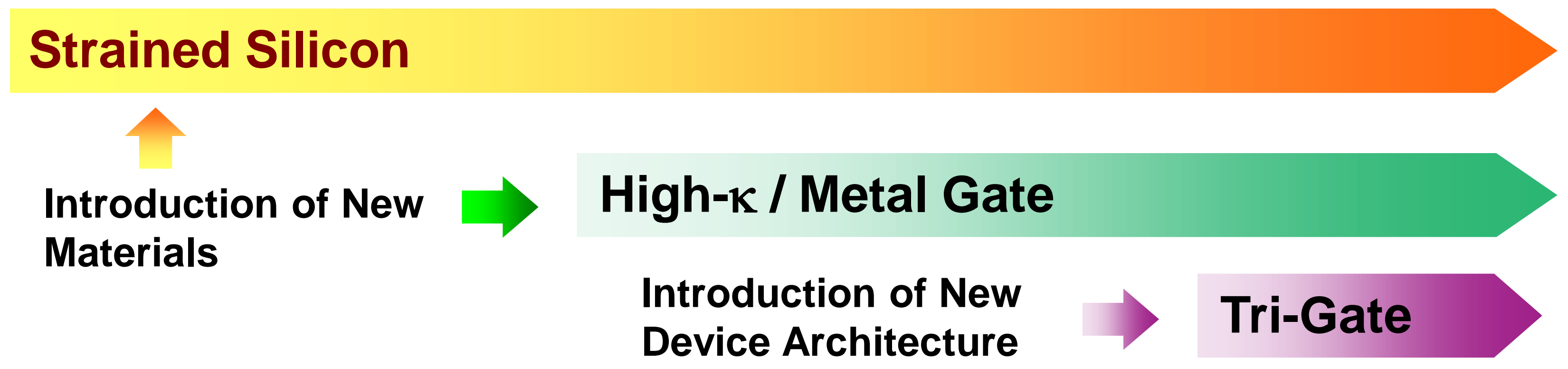
Industry Trends

- **System Drivers:**
  - Low and ultra-low power logic with multi-core/multi-modules
  - Dense 3D NVM RAM for Solid-State Disc (SSD) and dense DRAMs (TB)
  - High-level of functional integration (Digital, analog, RF, NVM, DRAM, MEMS, low power displays,…)
  - Faster data transfer needs between modules and between chips
- **Significant gaps – leads to device transitions**

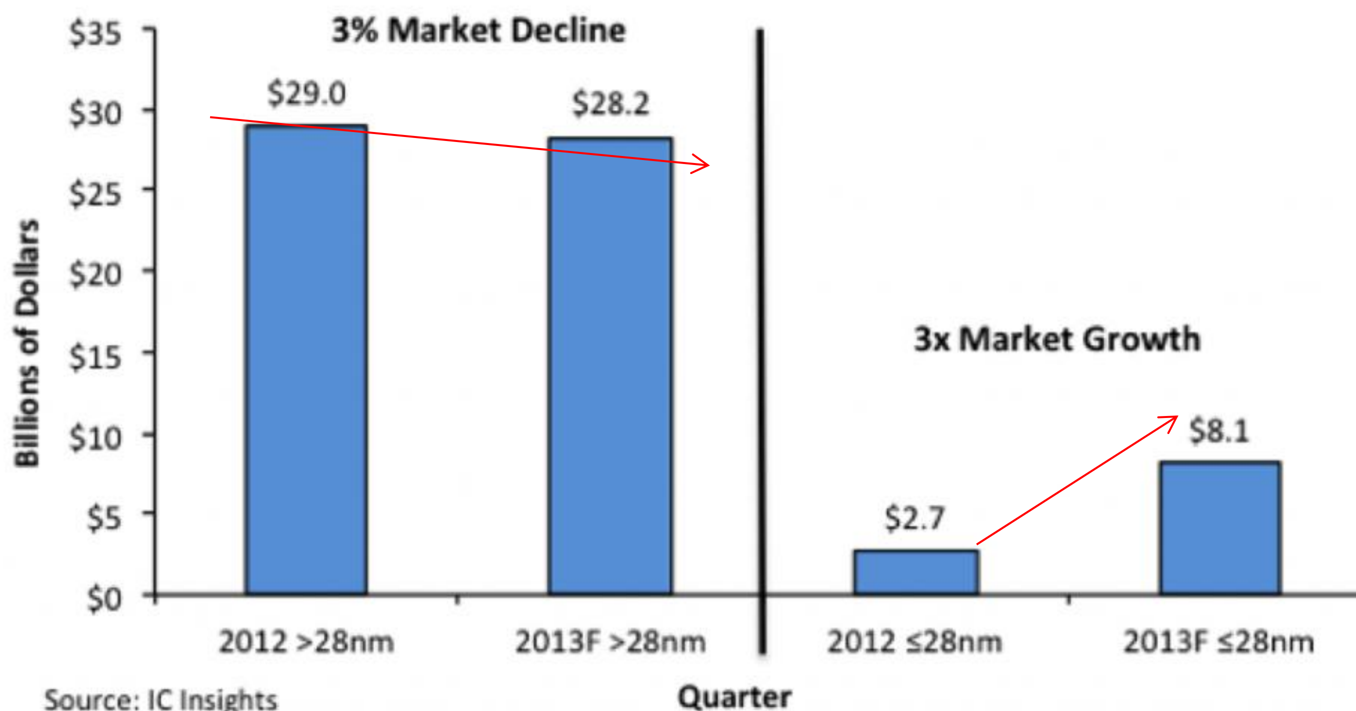
New materials & device architectures

Can we continue performance roadmap with litho scaling alone?





2013: Sub-28nm increasing in market growth



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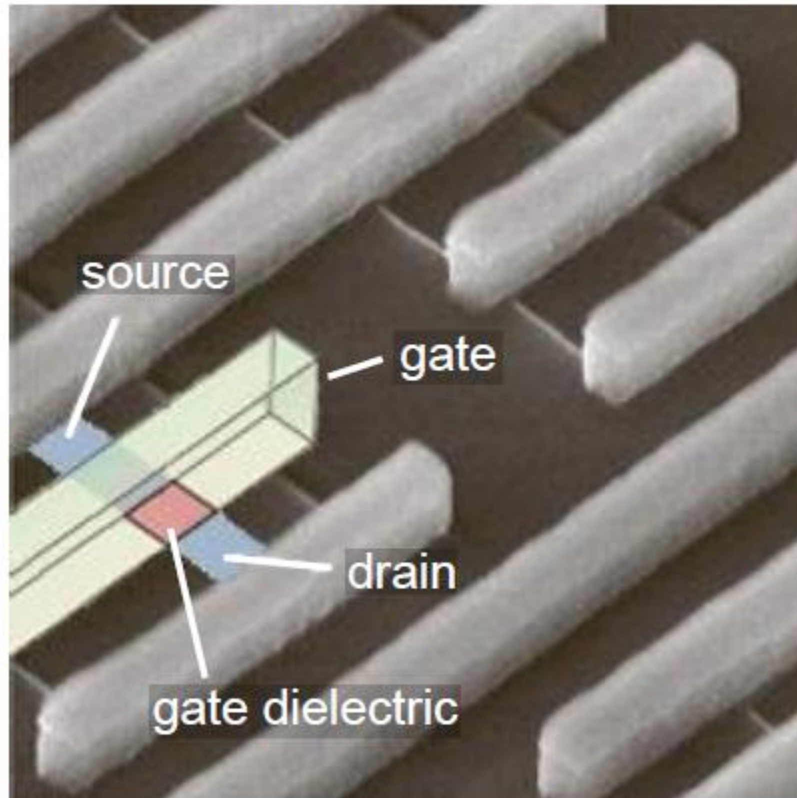
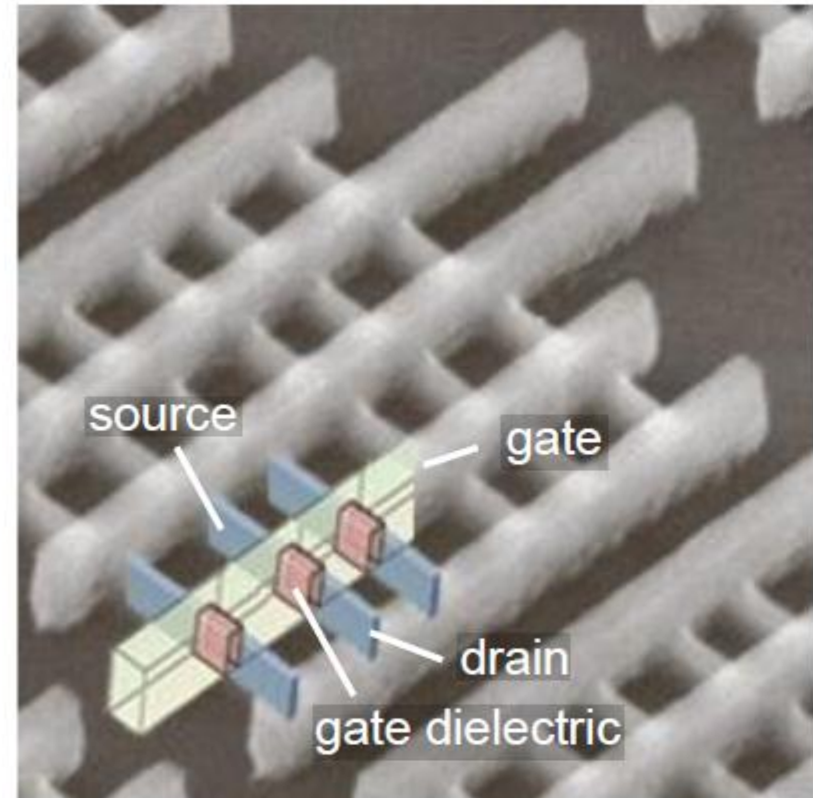


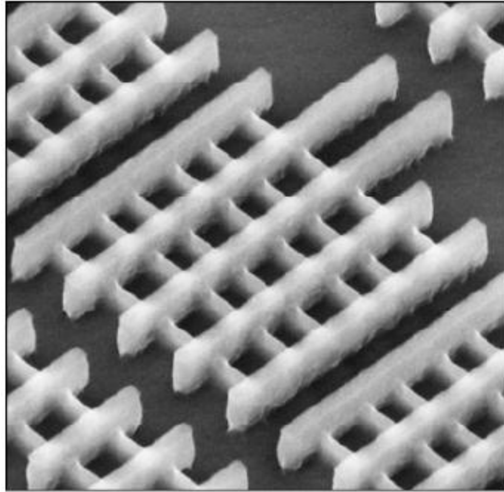


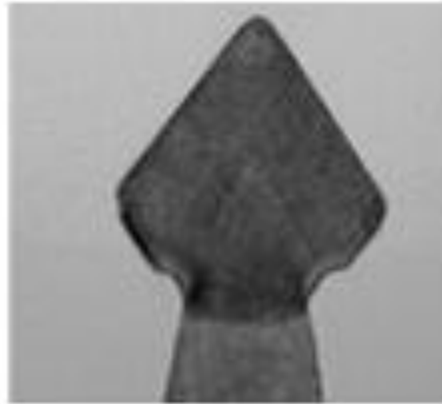
Gate dielectric shown in red

- Traditional→ planar
- Tri-gate → 3D

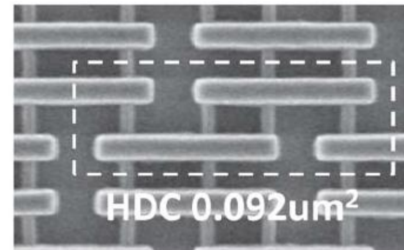
22nm Tri-Gate Announcements

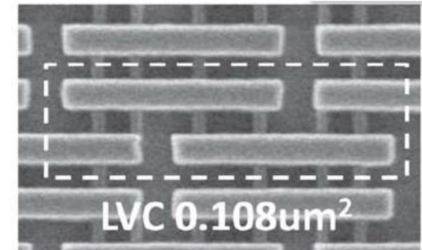
*Mark Bohr, Kaizad Mistry: Intel, April 25th, press release

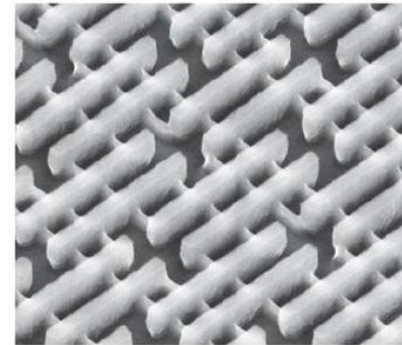




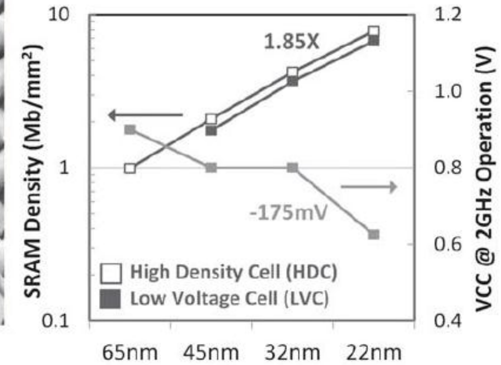
*ISSCC 2012, p229-230







22nm Tri-Gate LVC SRAM Array

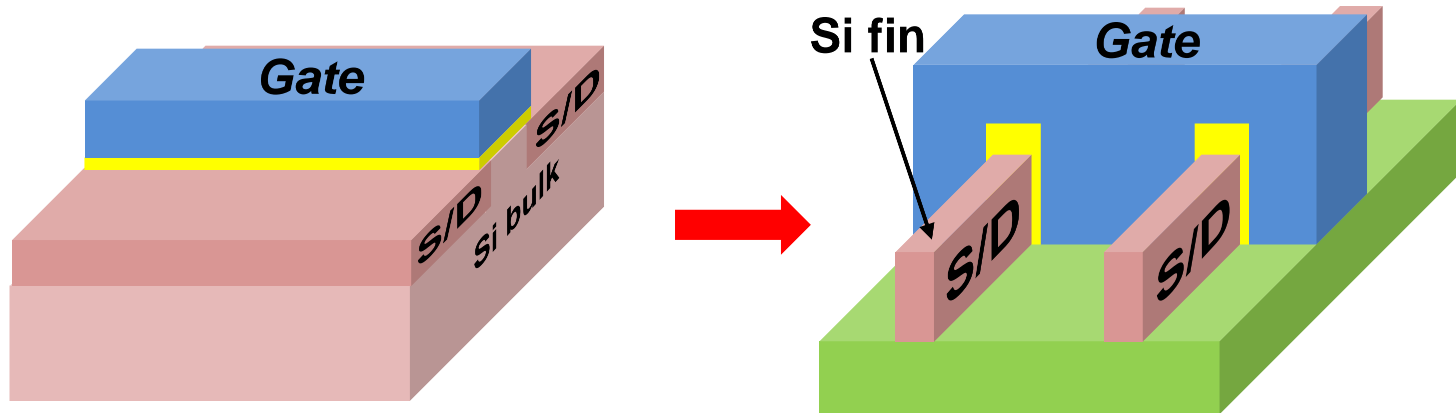


http://semimd.com/blog/2012/04/10/**finfets**-hkmg-on-2012-vlsi-symposium-program/

Issued by: TSMC
– Sept. 17, 2013 – “TSMC released Innovation 16FinFET systems-on-chip (SoC) designs……”

http://www.tsmc.com/tsmcdotcom/PRListingNewsAction.do?action=detail&newsid=8041&language=E

Improving Electrostatics: FinFETs



Conventional Planar FET **FinFET (Multi-Gate FET)**

1) Strong immunity to short-channel effects
   - supports smaller L_{eff} at same I_{off}
2) Better performance
   - supports smaller V_{TH} at same I_{off}
3) Low doping
   - supports higher μ & improved random dopant fluctuation

FinFET/tri-gate scaling challenges

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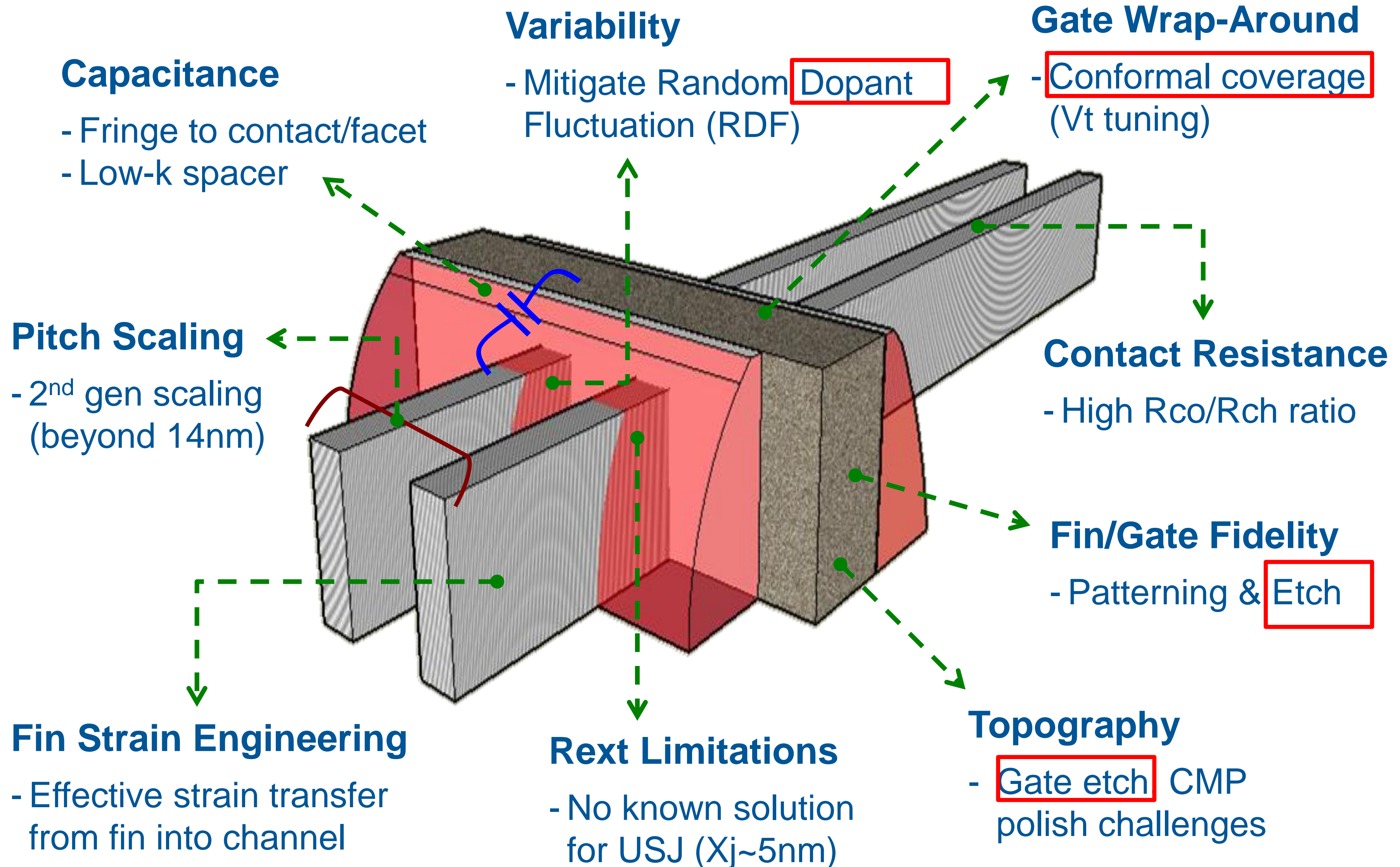
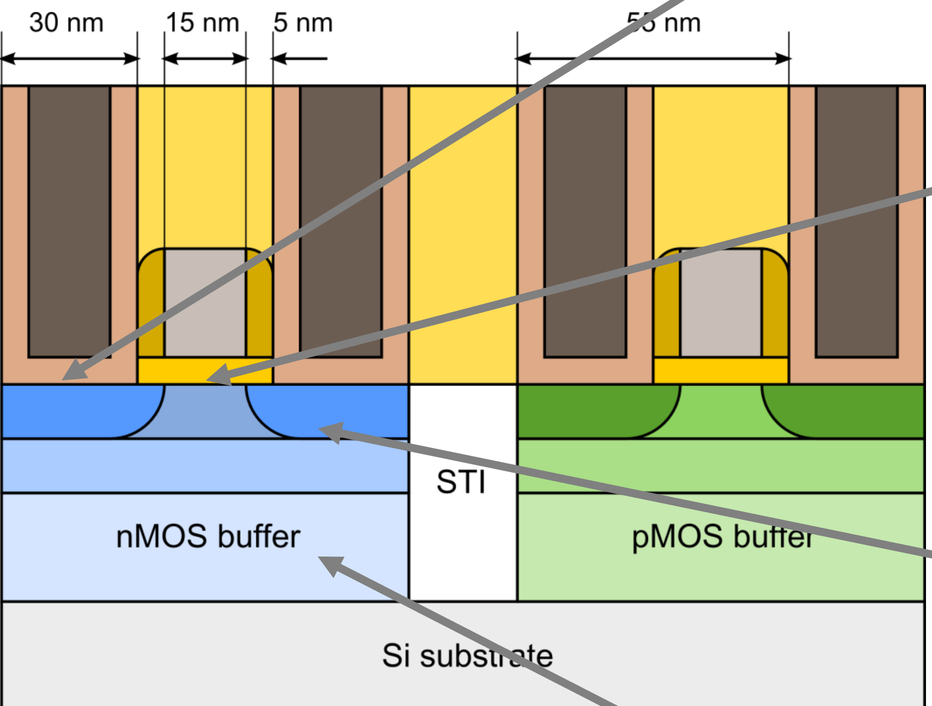


Non-Si (High-μ) Channel Materials

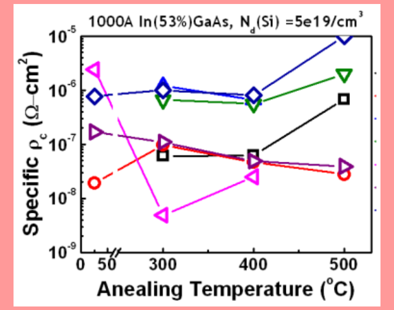
	Si	Ge	GaAs	InAs	InP	InSb
Electron mobility (cm^2/Vs)	1600	3900	9200	40000	5400	77000
Electron effective mass ($/m_o$)	m_t : 0.19 m_l : 0.916	m_t : 0.082 m_l : 1.467	0.067	0.023	0.082	0.014
Hole mobility (cm^2/Vs)	430	1900	400	500	200	850
Electron effective mass ($/m_o$)	m_{HH} : 0.49 m_{LH} : 0.16	m_{HH} : 0.28 m_{LH} : 0.044	m_{HH} : 0.45 m_{LH} : 0.082	m_{HH} : 0.57 m_{LH} : 0.35	m_{HH} : 0.45 m_{LH} : 0.12	m_{HH} : 0.44 m_{LH} : 0.016
Band gap (eV)	1.12	0.66	1.42	0.36	1.34	0.17
Permittivity	11.8	16	12	14.8	12.6	17

- **InGaAs : High electron mobility (light effective mass) → nMOSFET**
- **Ge : High hole mobility (light effective mass) → pMOSFET**
- **Band gap, permittivity & density of state ; negative effects**

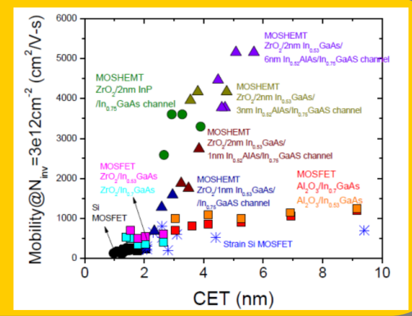
III-V: Lab to Fab
Module Development



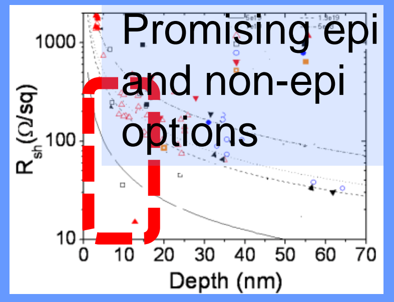
Au-free Contacts:
Thermal stability?, alignment? cleans…



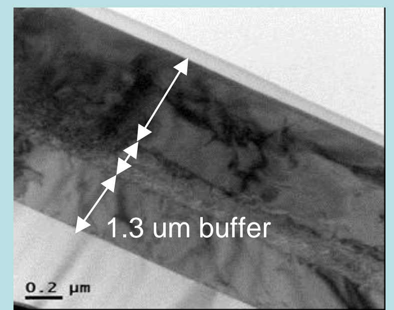
Scaled Gate Stacks:
Surface passivation?, Interface layer?, HKMG
Clustered tools ?



Defect-free Junctions:
Epi, I/I,
Plasma,
Monolayer Doping [MLD]

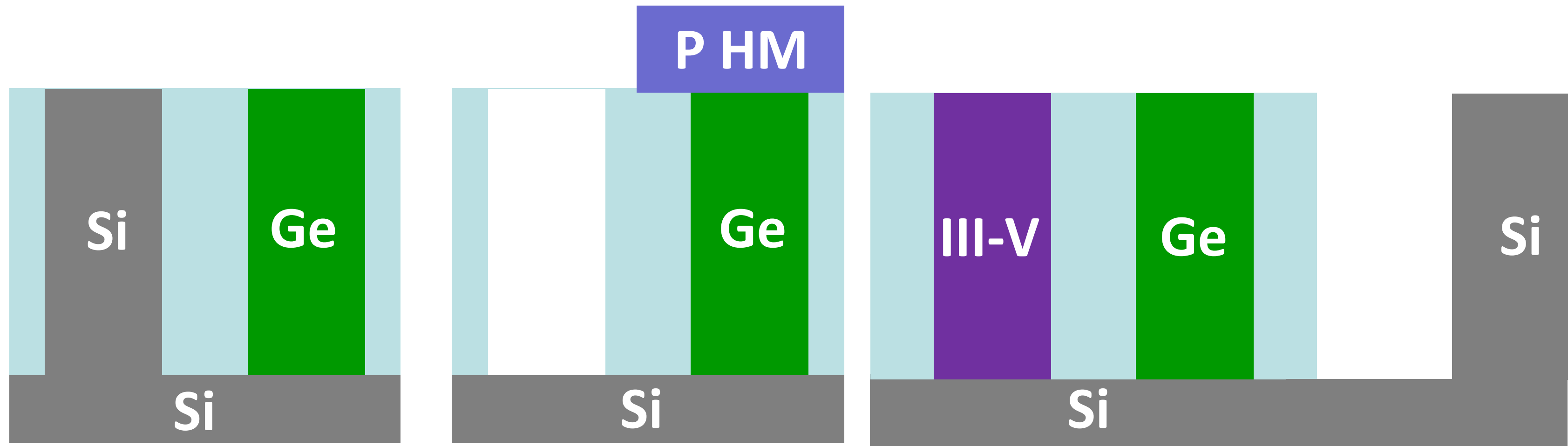


III-V on Si
Thin buffer?, XOI?
Large wafers ?

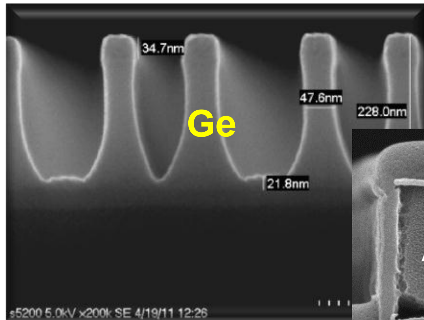


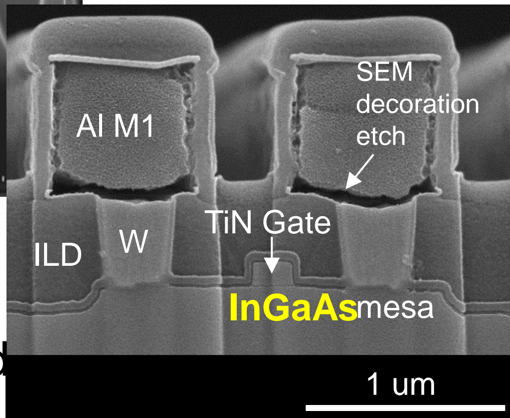
Heterointegration of Ge & III-V on Si for SOC

Three semiconductors on same chip!

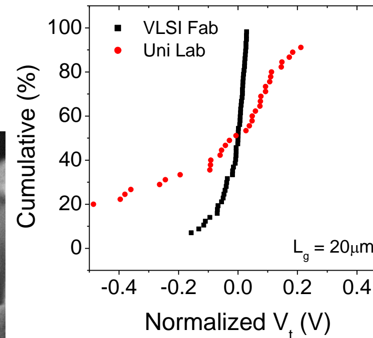


Ge on 300mm Si

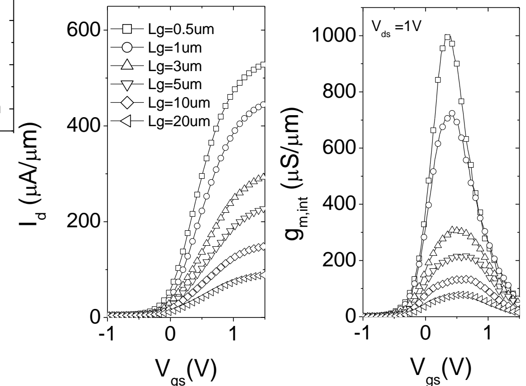




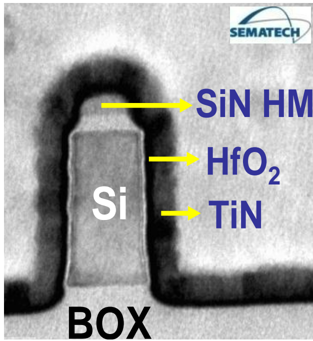
III-V on 200mm Si from standard VLSI fab



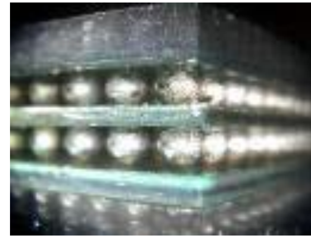
Improved uniformity/quality of III-V devices on 200mm Si



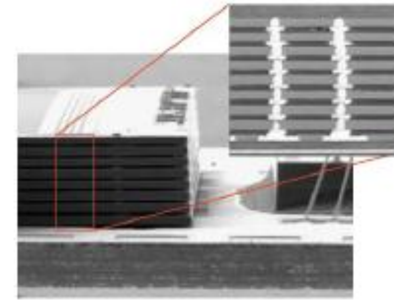
3D means different things to different people …



3D devices, Fin-FET, nano-wires, memory cell stacking

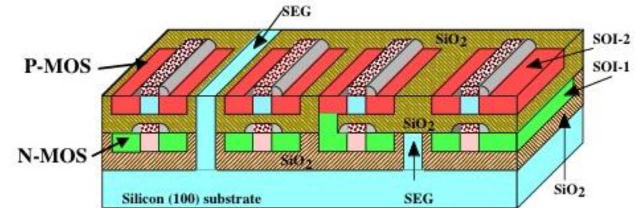


Non-TSV 3D packaging, package on package (PoP), through package via (TPV)



Source: Samsung

3D packaging with TSV

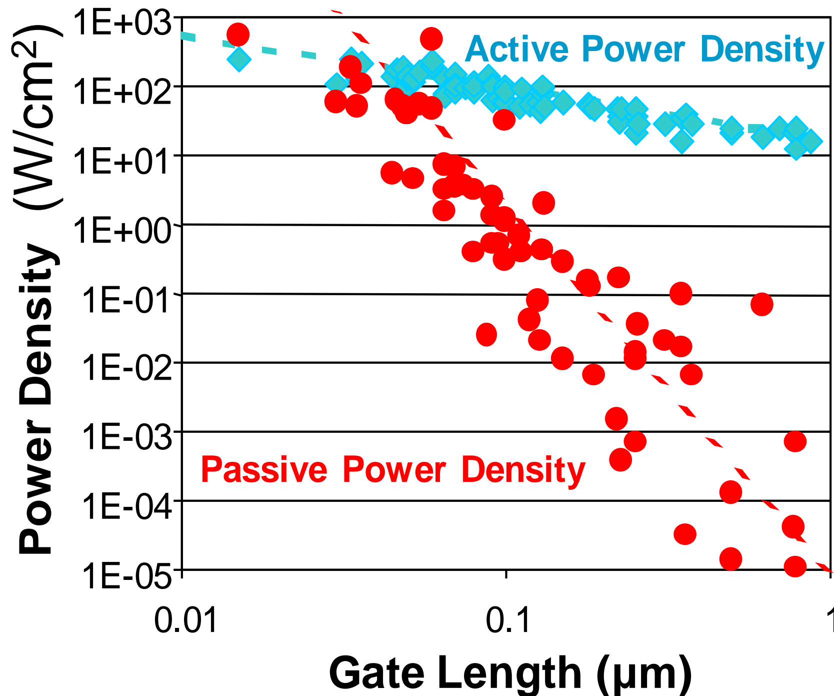


K Saraswat Stanford U.

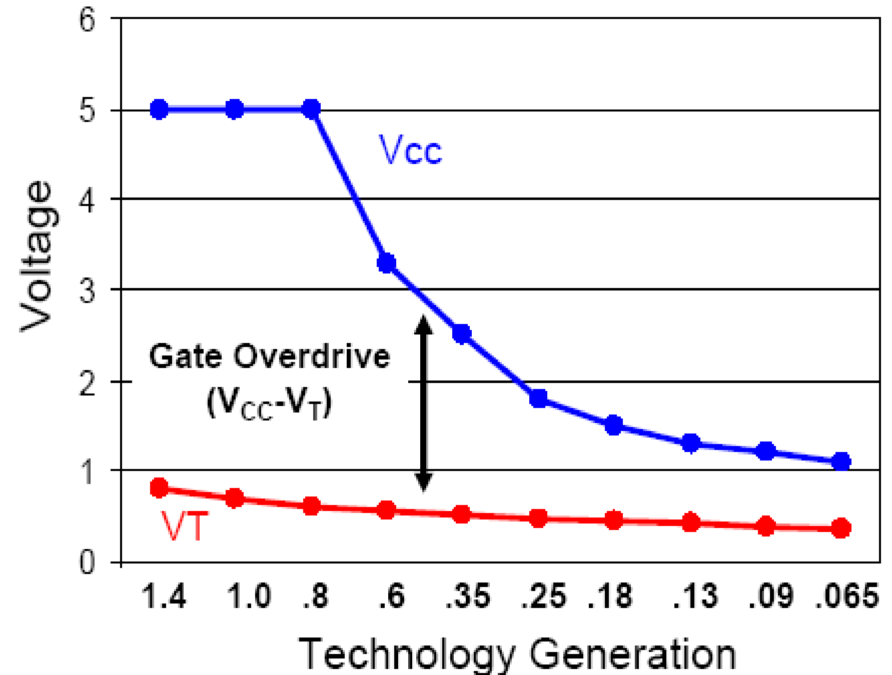
3D silicon integration

Power Management

The end of "traditional" scaling is near:
But→ Performance enhancement greatly increases power consumption.



(B. Meyerson et al., , IBM, Semico Conf., 2004)



(P. Packan (Intel), 2007 IEDM Short Course)

- Passive power has shown continuous increase due to V_{DD} scaling limit.
- V_{CC} scaling limited by V_T and subthreshold slope (which is kT/q limited)

→ need "green" devices not governed by kT/q ~ 60mV/dec limit.

Logic Device Roadmap

3D and Power Scaling is key

3D Architecture

Planar

High Volume Manufacturing

HKMG

3rd Gen SiGe

HKMG

4th Gen SiGe

PMOS

gate

SiGe S/D

channel

SiGe S/D

FinFET

HKMG

SiGe Strain

Vdd~1V

Si/Ge FinFETs

20 nm

SiGe

Si

QW finFETS

High-μ channel III-V/Ge FinFETs

Metal Gate / High-k

III-V

100 nm

III-V Devices on Si

III-V/Ge on Si

Nanowire FETs

Surround Gate

Ge

<100>

<110>

Al_2O_3

200 nm

SiO_2

Si Substrate

Strain

tFETs

Low Ion

Vdd~0.25V

Device Architecture
New Materials
Process Margin
RDF & Variability
Power vs performance
Circuit operation
Noise
Reliability

45nm 32nm 22nm 14nm 11nm 8nm <6nm

Power Performance Trade-offs

Beyond CMOS Opportunities → CMOS+

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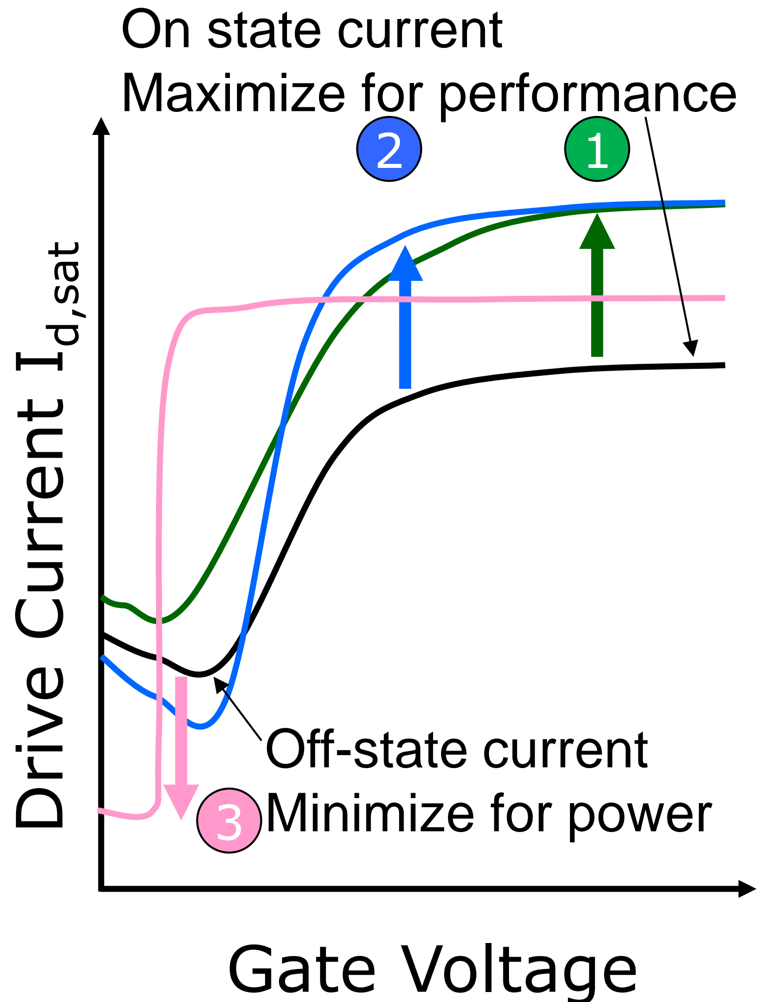

- High Mobility materials
  - SiGe, Ge, InGaAs
  - Graphene [μ_e ~15000 cm^2/V-s at RT]
- Better electrostatic control
  - Multiple gates + more channel area
  - FinFETs, nanowire FET
- Improve on-off ratio
  - Tunnel FET
    - Very steep ΔSS << 60 mV/dec
    - Low bias voltages (<< 1V)
  - Nano Electro Mechanical switch (NEMS)
    - Hybrid: I_{on} by CMOS + I_{off} by NEMS
    - Zero off-state leakage, Low Power

Logic and Memory Technology Scaling

Materials and novel structures driven

Advanced Materials | **Advanced Structures** | **Beyond CMOS Materials/Structures**

Logic

Bulk/SOI Si

Gate stack

High μ

Bulk/SOI Si

Channels, contacts, USJ

TaN

High-κ

Si

SiGe

2nm

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Metal

High-k

InGaAs

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High μ Fin/NW

Si

{100}

{100}

SiGe

Si

SiGe

High mobility Fins/Nanowires

20 nm

SiGe

Si

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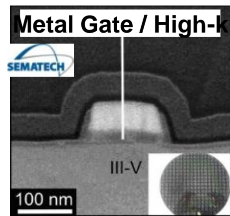
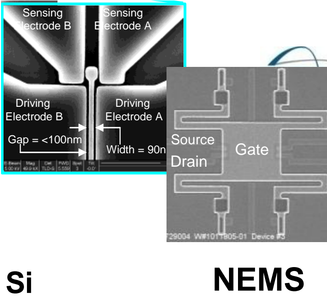
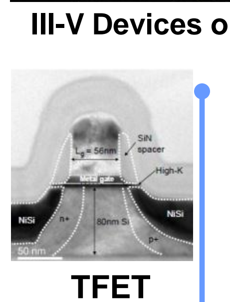


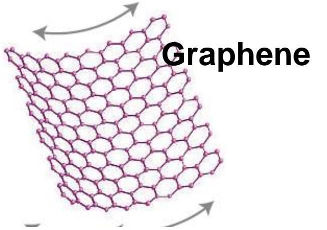
III-V Devices on Si



NEMS



TFET



2010 — 2020

Memory

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50nm

Bit Line

Source Line

SG

CG

PC

CT Flash

SEMATECH

TiN

W

WOx

W

TiN

RRAM

CMP'd

BE

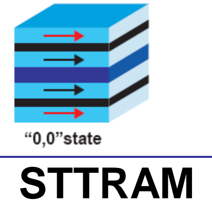
TE

HfOx

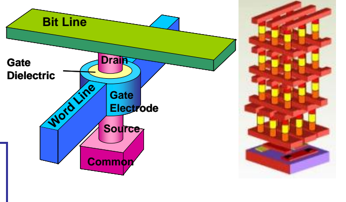
BE

RRAM Cross-point

<20nm RRAM



STTRAM



ReRAM/Nanowire 3DArray

Technology Trends: New Drivers

Communicate

Compute

Store

Display

Sense

Compute – MPU, GPU
Store – NAND, DRAM, NOR, SRAM
Communicate – WiFi, 3G/4G, BlueTooth
Sense – Orientation, GPS, Touch, …
Interface – HD, Touch, Voice commands, Camera

High Level of Functional Integration
Where-ever, When-ever, What-ever

Technology Trends: New Drivers

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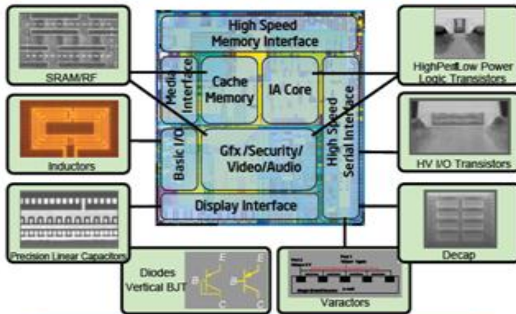
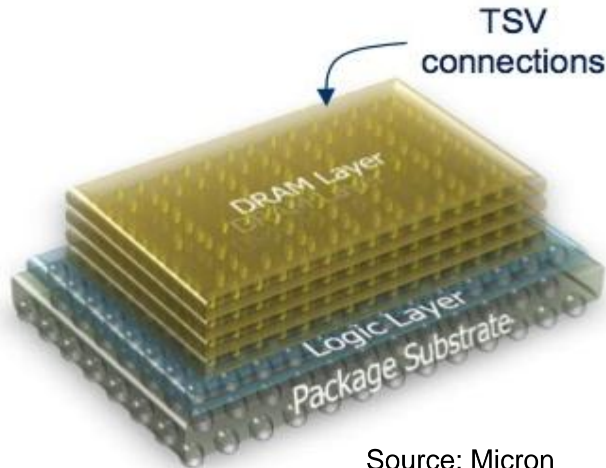


Source: Intel

System-on-a-Chip (SOC)

- Enables low power, low form factor solutions
- Minimal performance compromise
- Integrate MPU/GPU with analog, RF, NV memory
- High performance

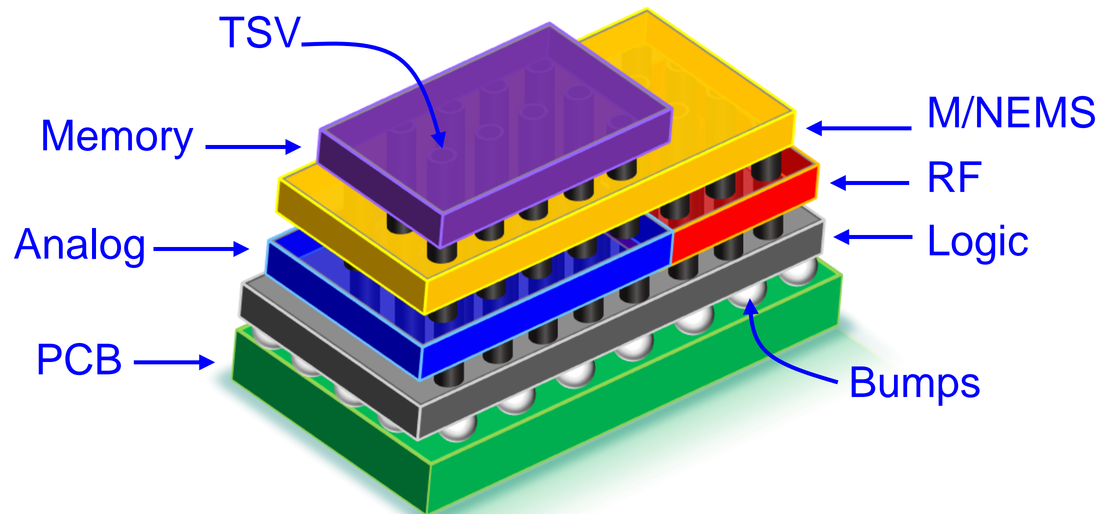


Source: Micron

System-in-a-Package (SIP)

- Enables low power, low form factor solutions
- Minimal performance compromise
- Integrate MPU/GPU with analog, RF, NV memory
- High bandwidth

Key Enabler: 3 Dimensional Integration (3DI)



- Transitioning into 3D technology will enable the continued proliferation of electronics into diverse domains.
- Further development is needed to meet the challenges of this transition;

3D Stacking

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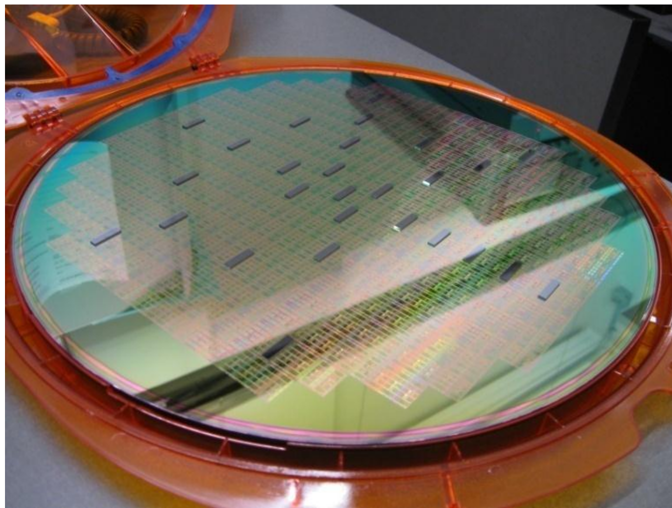
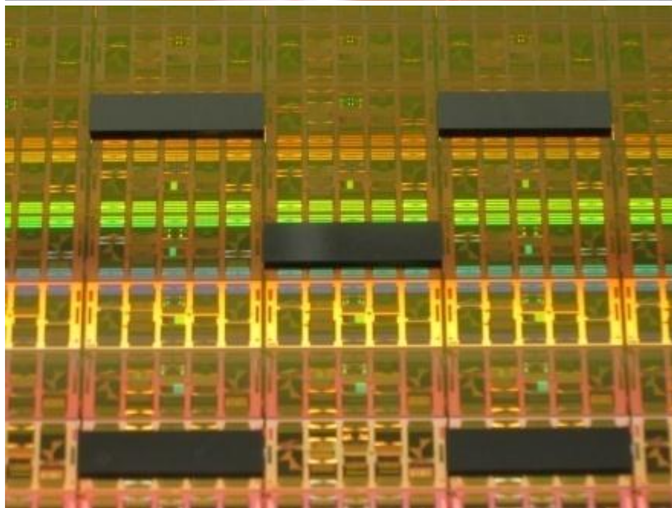
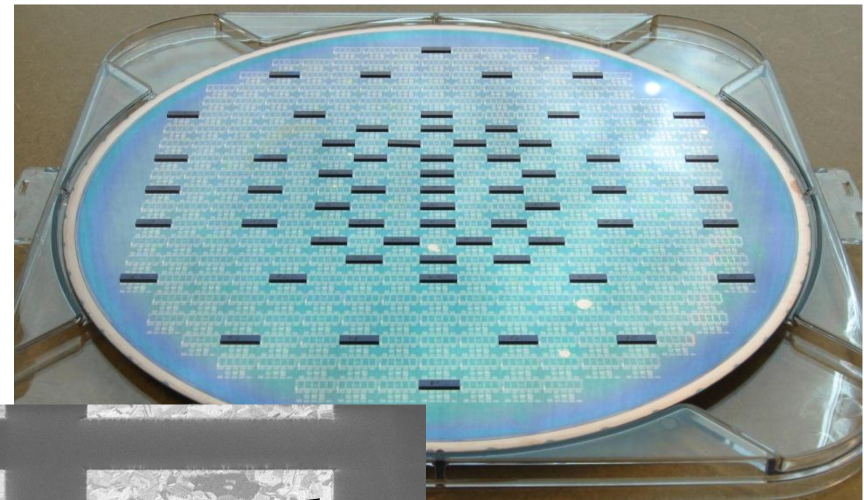
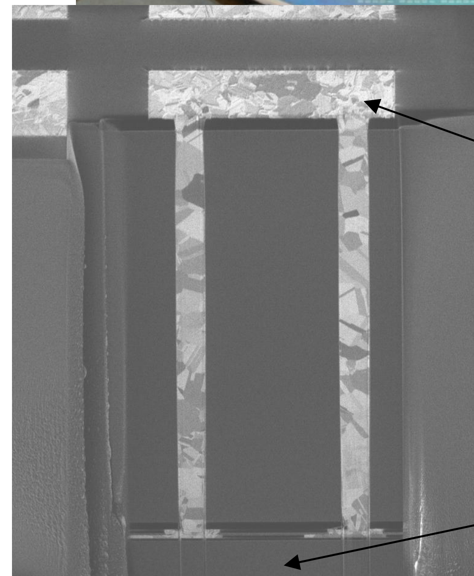
Enables system-level scaling of performance









Frontside metal

5x50 µm die-to-wafer TSV chain
(carrier wafer removed from top)

Cu-Cu bonded die

System on Chip Building Blocks – Adjacent Space

Eg: III-V introduction at 11nm node → photonics opportunity

Light Source

Modulator

Guide Light

CMOS

Photo-detection

Low-cost Assembly

P+
N+
P+
Ge PD
Si waveguide

Image courtesy: Intel

Vision of Future

Photodetector/ transimpedance amplifier
Flash memory
RAM
Microprocessor
CMOS/SOC
Waveguide
MEMS
Gallium arsenide laser diode
System-in-package (SIP)
Solder
Detector
OPTICAL
Transmitter
DIGITAL
Copper traces
RF
Decoupling capacitor
Microvia
Composite substrate

Source: Bryan Christie Designs

- **Use best suited material/device based on functional need**
- **Self-powered system in your pocket!**

Summary

- CMOS or Beyond CMOS is NOT the question
  - Sense, compute, store, transmit: Integrated functionality
- Convergence of technologies is the future
  - System level power reduction with performance gain is key
- Functional diversity vs device density
  - Focus of miniaturization shifts to adding diverse components
  - CMOS+ : Hybrid integration of beyond-CMOS with CMOS
  - Challenge: How can we fabricate them and make them work seamlessly
  - All systems are driven by mobile needs
- Logic and memory are 3D for density, performance/watt
- 3D Interconnects is a game changer
- Rich opportunity space for industry growth
  - Need for strong collaborative models to reduce risk and cost